MT6261D GSM GPRS SOC Processor Technical Brief

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1 System Overview

MT6261D is a monolithic chip integrating leading edge power management unit, analog baseband and radio circuitry based on the low-power CMOS process.

MT6261D is a feature-rich and extremely powerful single-chip solution for high-end GSM/GPRS capability. Based on the 32-bit ARM7EJ-S^{TM} RISC processor, MT6261D's superb processing power, along with high bandwidth architecture and dedicated hardware support, provides a platform for high-performance GPRS Class 12 MODEM application and leading-edge multimedia applications.

MT6261D also features:

- A highly integrated Bluetooth transceiver which is fully compliant with Bluetooth specification v3.0.
- A FM receiver supporting both audio broadcast de-modulation and RDS/RBDS data decoding.

Typical application diagram is shown in **Figure 1**.

Platform

MT6261D is capable of running the ARM7EJ-S^{TM} RISC processor, which provides the best trade-off between system performance and power consumption.

For large amounts of data transfer, high-performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing the MCU processing load.

Targeted as a media-rich platform for mobile applications, MT6261D also provides hardware security digital rights management for copyright protection. For further safeguard and to protect the manufacturer's development investment, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Memory

MT6261D supports serial flash interface with various operating frequencies.

Multimedia

The MT6261D multimedia subsystem provides serial interface for CMOS sensors. The camera resolution is up to VGA size. The software-based codec can be used to process various video types. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT6261D is implemented with a high-performance audio synthesis technology, as well as a high-quality audio amplifier to provide superior audio experiences.

Connectivity and storage

MT6261D supports UART, USB 1.1 FS/LS , SDIO and SD storage systems. These interfaces provide MT6261D users with the highest level of flexibility in implementing high-end solutions.

To achieve a complete user interface, MT6261D also brings together all the necessary peripheral blocks for a multimedia GSM/GPRS phone. The peripheral blocks include the keypad scanner with the capability to detect multiple key presses, SIM controller, real-time clock, PWM, serial LCD

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controller and general-purpose programmable I/Os.

Audio

Using a highly integrated mixed-signal audio front-end, the MT6261D architecture provides easy audio interfacing with direct connection to the audio transducers. The audio interface integrates A/D converters for voice band, as well as high-resolution stereo D/A converters for both audio and voice band.

MT6261D supports AMR codec to adaptively optimize the quality of speech and audio. Moreover, HE-AAC codec is implemented to deliver CD-quality audio at low bit rates.

In addition, an 1.2W audio amplifier is also embedded to save the BOM cost of adopting external amplifiers.

GSM/GPRS radio

MT6261D integrates a mixed-signal baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. The front-end contains gain and offset calibration mechanisms and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT6261D achieves outstanding MODEM performance by utilizing a highly dynamic range ADC in the RF downlink path.

MT6261D embeds a high-performance and completely integrated single-ended SAW-less RF transceiver for multi-band GSM cellular system. In this RF transceiver, a quad-band receiving feature with high sensitivity is supported utilizing one RF receiver and a fully integrated channel filter. With ultra-high dynamic range, the off-chip balun and SAW filters on the receiving path can be removed for BOM cost reduction. In addition, the minimum component count is guaranteed by realizing a highly integrated transmitter, low-spur frequency synthesizer and a Digitally-Controlled Crystal Oscillator (DCXO).

Bluetooth radio

MT6261D offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components are required. MT6261D provides superior sensitivity and class 1 output power and thus ensures the quality of the connection with a wide range of Bluetooth devices.

MT6261D is fully compliant with Bluetooth v3.0 and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with 802.11 system.

MT6261D supports rich Bluetooth profiles, enabling diversified applications that are widely used on the handset with excellent interoperability.

FM radio

The FM radio subsystem provides a completely integrated FM Rx receiver supporting 65 ~ 108MHz FM bands with 50kHz tuning step. In addition to receiving FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM transceiver utilizes state-of-the-art digital demodulation/modulation techniques to achieve excellent performance.

In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize Rx system performance in all ranges of signal quality by reference of a very sophisticated channel quality index (CQI). When the received signal quality is poor, the design not only enhances the ACI rejection capability

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but also uses a very ingenious skill to soft mute annoying noise so as to provide good perception quality.

The FM radio subsystem supports both long antenna, which is usually an earphone, and auto-calibrated short antenna, which is usually a FPC short antenna or shared antenna with GSM for different application scenarios.

Debugging function

The JTAG interface enables in-circuit debugging of the software program with the ARM7EJ-S™ core. With this standardized debugging interface, MT6261D provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Power management

A power management is embedded in MT6261D to provide rich features a high-end feature phone supports, including Li-ion battery charger, high performance and low quiescent current LDOs, and drivers for LED and backlight.

MT6261D offers various low-power features to help reduce the system power consumption. MT6261D is also fabricated in an advanced low-power CMOS process, hence providing an overall ultra-low leakage solution.

Package

The MT6261D device is offered in a 8.1mm×7.6mm, 145-ball, 0.5mm pitch, TFBGA package.

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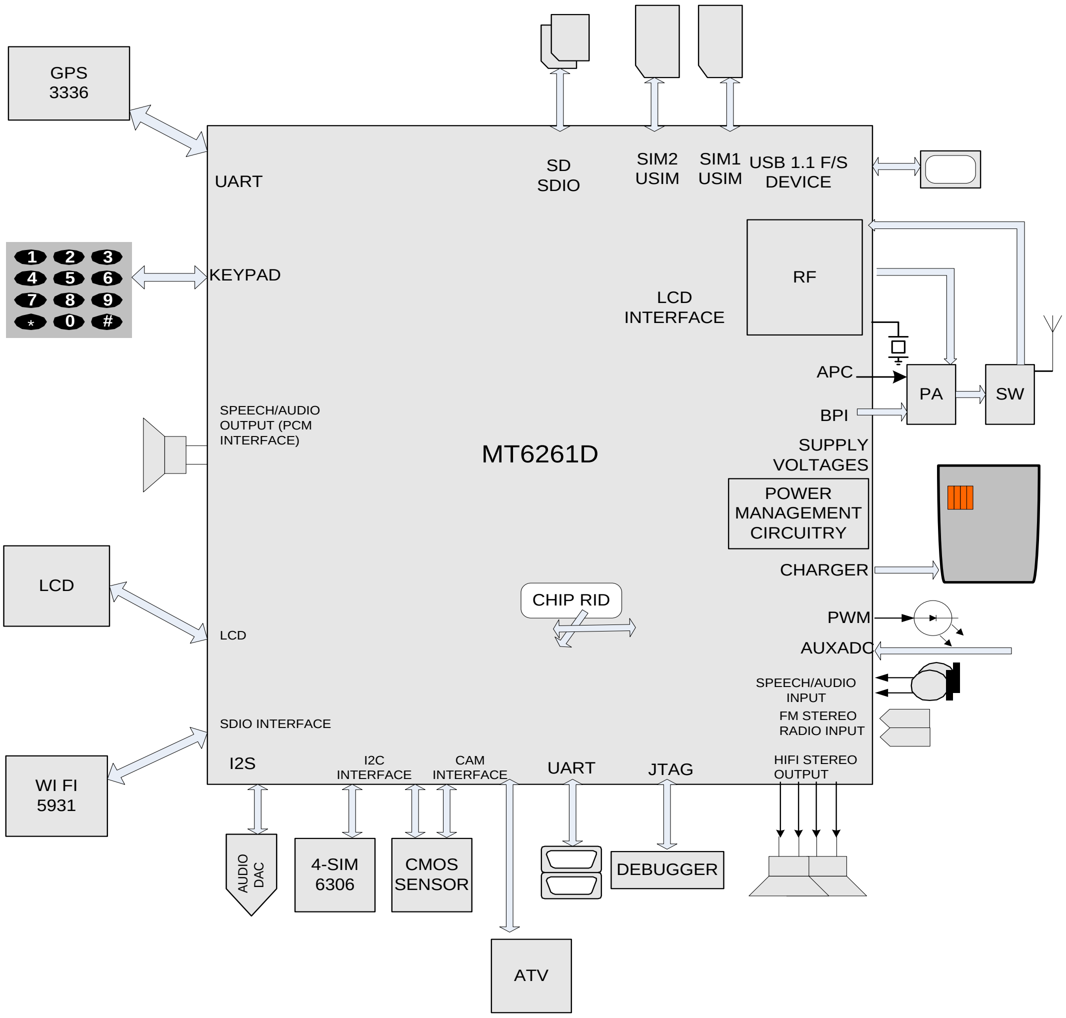

Figure 1. Typical application of MT6261D

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1.1 Platform Features

General

- Integrated voice-band, audio-band and base-band analog front-end
- Integrated full-featured power management unit

MCU subsystem

- ARM7EJ-S™ 32-bit RISC processor
- Java hardware acceleration for fast Java-based games and applets
- High-performance multi-layer AHB bus
- Dedicated DMA bus with 16 DMA channels
- On-chip boot ROM for factory flash programming
- Watchdog timer for system crash recovery
- 3 sets of general-purpose timers
- Circuit switch data coprocessor
- Division coprocessor

User interfaces

- 5-row x 5-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- Dual SIM/USIM controller with hardware T = 0/T = 1 protocol control
- Real-time clock (RTC) operating with a low-quiescent-current power supply
- General-purpose I/Os (GPIOs) available for auxiliary applications
- 2 sets of Pulse Width Modulation (PWM) output
- 24 external interrupt lines
- 1 external channel auxiliary 10-bit A/D converter

Security

- Supports security key and chip random ID

Connectivity

- 3 UARTs with hardware flow control and supports baud rate up to 921,600 bps
- FS/LS USB 1.1 device controller
- Multimedia card, secure digital Memory Card, host controller with flexible I/O voltage power
- Supports 4-bit SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for audio applications
- I2C master interface for peripheral management including image sensors
- SPI master/slave interface for peripheral management.

Power management

- Li-ion battery charger
- 13 LDOs for the power supply of memory card, camera, Bluetooth, RF, SIM card and other diversified usage
- 1 open-drain output switches to supply/control the LED
- LDO type vibrator
- One NMOS switch to control keypad LED
- Thermal overload protection
- Under-voltage lock-out protection
- Over-voltage protection
- Different levels of power-down modes with sophisticated software control enables excellent power saving performance.

Test and debugging

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- Built-in digital and analog loop back modes for both audio and baseband front-end
- DAI port complies with GSM Rec.11.10.
- JTAG port for debugging embedded MCU

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1.2 MODEM Features

Radio interface and baseband front-end

- Digital PM data path with baseband front-end
- High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
- 10-bit D/A converter for Automatic Power Control (APC)
- Programmable radio Rx filter with adaptive gain control
- Dedicated Rx filter for FB acquisition
- 6-pin Baseband Parallel Interface (BPI) with programmable driving strength
- Supports multi-band

Voice and modem CODEC

- Dial tone generation
- Voice memo
- Noise reduction
- Echo suppression
- Advanced sidetone oscillation reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- Supports GSM/GPRS modem
- GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS GEA1, GEA2 and GEA3 ciphering
- GPRS packet switched data with CS1/CS2/CS3/CS4 coding schemes
- GPRS Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS(Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec.

Voice interface and voice front-end

- Microphone input has one low-noise amplifier with programmable gain and Automatic Gain Control (AGC) mechanisms
- Voice power amplifier with programmable gain
- 2nd order Sigma-Delta A/D converter for voice uplink path
- Shares D/A converter with audio playback path
- Supports full-duplex hands-free operation
- Compliant with GSM 03.50

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1.3 GSM/GPRS RF Features

Receiver

- Dual single-ended LNAs support Quad bandQuadrature RF mixer
- Fully integrated channel filter
- High dynamic range ADC
- 12dB PGA gain with 6dB gain step

Transmitter

- Transmitter outputs support quad bands.
- Highly precise and low noise RF transmitter for GSM/GPRS applications

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GPRS applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Low power mode supports 32K crystal removal

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1.4 Multimedia Features

LCD controller

- Supports simultaneous connection to seral 2 lane LCD modules
- LCM formats supported: RGB565, RGB666, RGB888
- Supports LCD module with maximum resolution up to 320x240
- Per pixel alpha channel
- True color engine
- Supports hardware display rotation
- Capable of combining display memories with up to 4 blending layers

Camera interface

- YUV422 format image input
- Capable of processing image of size up to VGA (Mediatek serial interface)

JPEG decoder

- Baseline JPEG decoding
- Supports various YUV formats, DC/AC Huffman tables and quantization tables

JPEG encoder

- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 compliance
- Supports YUV420 and grayscale formats
- Supports EXIF/JFIF
- Standard DC and AC Huffman tables
- Provides 5 levels of encode quality
- Supports zeros shutter delay

MJPEG

- Decode spec: CIF@30fps
- Encode spec: QVGA@15fps

Image data processing

- Supports 4x digital zoom
- High throughput hardware scaler. Capable of tailoring an image to an arbitrary size.
- Horizontal scaling with bilinear interpolation
- Vertical scaling with bilinear interpolation
- YUV and RGB color space conversion
- RGB/YCbCr format thumbnail output

MPEG-4/H.263 CODEC

- Software-based MPEG4 encoder
- Software-based MPEG4 decoder
- ISO/IEC 14496-2 simple profile:
  - Decode spec: 480x320@25fps
  - Encode spec: QVGA@15fps
- ISO/IEC 14496-2 advanced simple profile:
  - Decode @ level 0/1/2/3
  - ITU-T H.263 profile 0 @ level 40
- Supports visual tools for decoder: I-VOP, P-VOP, B-VOP, AC/DC prediction, 4-MV, unrestricted MV, error resilience, short header, global motion compensation, method 1/2 quantization, quarter-pel motion compensation.
- Error resilience for decoder: Slice resynchronization, data partitioning, reversible VLC
- Supports visual tools for encoder: I-VOP, P-VOP, Half-Pel, DC prediction, unrestricted MV, short header

H.264

- ISO/IEC 14496-10 baseline profile
  - Decode spec: QCIF@30fps

2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565, 24-bpp ARGB6666.

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- 4 layers overlay with individual color format, window size, source key, constant alpha and rotation
- Rectangle fill with constant
- BitBlt: Capable with 7 rotation types
- Alpha blending with 7 rotation types, per-pixel alpha and pre-multiplied alpha
- Font drawing: Normal font and anti-aliasing font

Audio CODEC

- Supports AAC codec decoding
- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set of 128 instruments and 47 sets of percussions
- PCM playback and record
- Digital audio playback

Audio interface and audio front-end

- Supports I2S interface
- High-resolution D/A converters for stereo audio playback
- Voice band A/D converter support
- Stereo to mono conversion

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1.5 Bluetooth Features

Radio features

- Fully compliant with Bluetooth specification 3.0
- Low out-of-band spurious emissions support simultaneous operation with GPS and GSM/GPRS worldwide radio systems
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and Balun
- Fully integrated PA provides 7.5dBm output power
- -95dBm sensitivity with excellent interference rejection performance
- Hardware AGC dynamically adjusts receiver performance in changing environments

Baseband features

- Up to 4 simultaneous active ACL links
- Up to 1 simultaneous SCO or eSCO link with CVSD coding
- Supports eSCO
- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan
- Supports sniff mode
- AFH and PTA collaborative support for WLAN/BT coexistence
- Idle mode and sleep mode enables ultra-low power consumption.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption
- Channel quality driven data rate adaptation
- Channel assessment for AFH

Platform features

- Embedded processor for Bluetooth protocol stack with built-in memory system
- Fully verified ROM based system with code patch for feature enhancement

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1.6 FM Features

- 65-108MHz worldwide FM bands with 50KHz tuning step
- Supports RDS/RBDS radio data system
- Digital stereo demodulator
- Adaptive FM demodulator for both high- and low-quality scenarios
- Low sensitivity level with superior interference rejection
- Programmable de-emphasis (bypass/50 S/75 S)
- Stereophonic multiplex signal (MPX) signal detection and demodulation
- Superior stereo noise reduction and soft mute volume control
- Audio dynamic range control
- Mono/stereo blending
- Audio sensitivity3dBµVemf (SINAD=26dB)
- Audio SINAD≥60dB
- Supports Anti-jamming algorithm
- Supports short antenna

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1.7 General Descriptions

Figure 2 is the block diagram of MT6261D. Based on a multi-processor architecture, MT6261D integrates an ARM7EJ-S^{TM} core, the main processor running high-level GSM protocol software as well as multimedia applications, single digital signal processor core, which manages the low-level MODEM and advanced audio functions, an embedded processor running Bluetooth baseband and link control protocol and the Bluetooth radio control.

MT6261D consists of the following subsystems:

- Microcontroller Unit (MCU) subsystem: Includes an ARM7EJ-S^{TM} RISC processor and its accompanying memory management and interrupt handling logics
- Digital Signal Processor (DSP) subsystem: Includes a DSP and its accompanying memory, memory controller and interrupt controller
- MCU/DSP interface: Junction at which the MCU and the DSP exchange hardware and software information
- Microcontroller peripherals: Include all user interface modules and RF control interface modules
- Microcontroller coprocessors: Run computing-intensive processes in place of the microcontroller
- DSP peripherals: Hardware accelerators for GSM/GPRS channel codec
- Multimedia subsystem: Integrates several advanced accelerators to support multimedia applications
- Voice front-end: Data path for converting analog speech to and from digital speech
- Audio front-end: Data path for converting stereo audio from an audio source
- Baseband front-end: Data path for converting a digital signal to and from an analog signal from the RF modules
- Timing generator: Generates the control signals related to the TDMA frame timing
- Power, reset and clock subsystem: Manage the power, reset and clock distribution inside MT6261D.
- Bluetooth subsystem: Includes an embedded processor with embedded ROM/RAM system, baseband processor, and a high-performance radio block
- Power management unit: Self-contained power supply source which also controls the charging and system startup circuitry.

Details of the individual subsystems and blocks are described in the following chapters.

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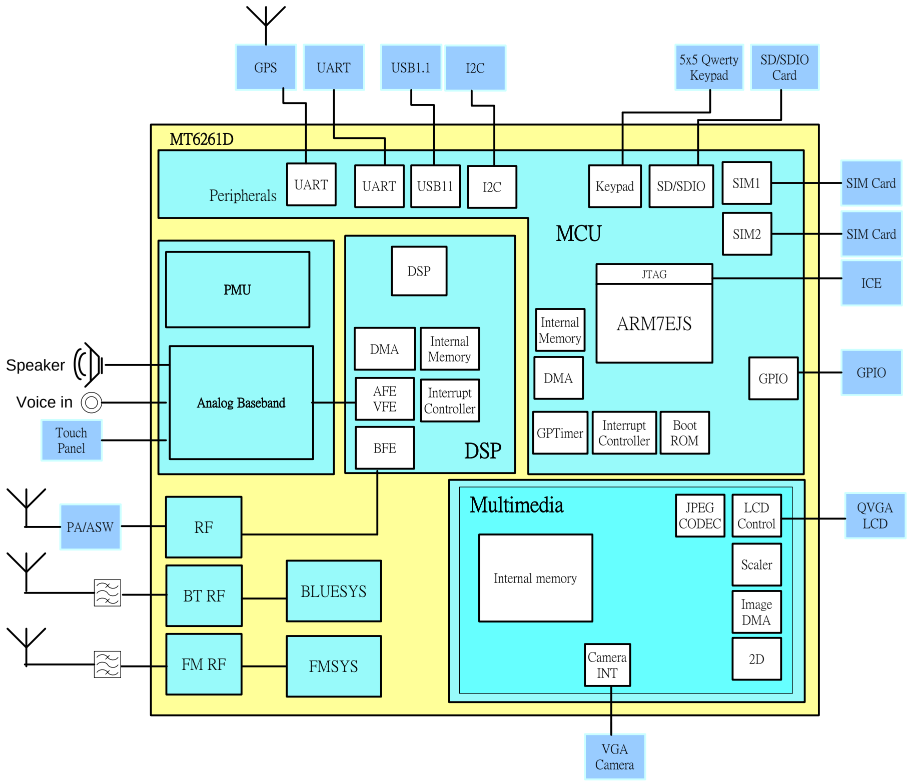

Figure 2. MT6261D block diagram

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2 Product Descriptions

2.1 Pin Description

2.1.1 Ball Diagram

For MT6261D, an TFBGA 8.1mm*7.6mm, 145-ball, 0.5mm pitch package is offered. Pin-outs and the top view are illustrated in **Figure 3** for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	RXLB	AVSS_2G	XTAL1	XTAL2		AVSS_BT	BT_LNA		BPI_BUS2	CMCSD0		CMRST	KCOL1		KROW1	KROW0	A
B		RXHB	EINT	AVSS_2G	GPIO_11	FREF	AVSS_BT	BPI_BUS1	BPI_BUS0	CMMCLK	CMCSK	CMPDN	KCOL0		KROW2		B
C	TX_LB	AVSS_2G			SRCLKENAI			AVDD15_BTRF	CMCSD1			VDDK	KCOL2	KCOL3	KROW3	KROW4	C
D	AVSS_2G	TX_HB		GPIO_10	EXT_CLK_SEL			VIO28	SDA28			GND		KCOL4	URXD1	UTXD1	D
E		AVSS44_ALDO			VRF			SCL28	GND			GND	GND	GPIO_0	GPIO_1		E
F	AVSS_FM	FM_ANT_P								GND					GPIO_2	GPIO_3	F
G	VREF	PWRKEY	VBAT_VA	VCAMA	TESTMODE	AVSS44_ALDO	GND	GND	GND						GPIO_5	GPIO_4	G
H		CHRLDO	BATSNS	ISENSE				GND	GND			GPIO_9	GPIO_8	GPIO_7	GPIO_6		H
J	VCDT	BATON							GND			GND	RESETB	VSF	LSCE_B	LSRSTB	J
K	DRV	KPLED	ISINK							GND					LSDA	LSCK	K
L		AVSS44_PMU		AVDD25_V2P5			AU_MICBIAS0	ACCDET		AVSS44_DLDO					LSA0		L
M	SPK_OUTN	AVSS_SPK		VSBST	VSBST		AU_VIN0_P	APC			SIM1_SIO	VIO18	SIM2_SIO	VSIM2	LPTE	SIM2_SRST	M
N	SPK_OUTP	AVSS_SPK		AVSS44_BOOST	AVSS44_BOOST		AU_VIN0_N	AUXIN4			VUSB		MCDA3	MCCM0	MCDA1	SIM2_SCLK	N
P		AVDD_SPK		VSBST_OUT	AVSS28_ABB	AU_VIN1_P	AU_VIN1_N	VCORE	VRTC	USB11_DM	USB11_DP	SIM1_SCLK	MCDA2		MCDA0		P
R	AU_HPR	AU_HPL	AU_HSP	AU_HSN	VA		AVSS28_ABB		VBAT_DIGITAL	VIBR		SIM1_SRST	VSIM1		MCCK	VMC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. Ball diagram and top view

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2.1.2 Pin Coordination

Table 1. Pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	RXLB	D16	UTXD1	J1	VCDT
A10	CMCSD0	D2	TX_HB	J12	GND
A12	CMRST	D4	GPIO_10	J13	RESETB
A13	KCOL1	D5	EXT_CLK_SEL	J14	VSF
A15	KROW1	D8	VIO28	J15	LSCE_B
A16	KROW0	D9	SDA28	J16	LSRSTB
A2	AVSS_2G	E12	GND	J2	BATON
A3	XTAL1	E13	GND	J9	GND
A4	XTAL2	E14	GPIO_0	K1	DRV
A6	AVSS_BT	E15	GPIO_1	K10	GND
A7	BT_LNA	E2	AVSS44_ALDO	K15	LSDA
A9	BPI_BUS2	E5	VRF	K16	LSCK
B10	CMMCLK	E8	SCL28	K2	KPLED
B11	CMCSK	E9	GND	K3	ISINK
B12	CMPDN	F1	AVSS_FM	L10	AVSS44_DLDO
B13	KCOL0	F10	GND	L15	LSA0
B15	KROW2	F15	GPIO_2	L2	AVSS44_PMU
B2	RXHB	F16	GPIO_3	L4	AVDD25_V2P5
B3	EINT	F2	FM_ANT_P	L7	AU_MICBIAS0
B4	AVSS_2G	G1	VREF	L8	ACCDET
B5	GPIO_11	G15	GPIO_5	M1	SPK_OUTN
B6	FREF	G16	GPIO_4	M11	SIM1_SIO
B7	AVSS_BT	G2	PWRKEY	M12	VIO18
B8	BPI_BUS1	G3	VBAT_VA	M13	SIM2_SIO
B9	BPI_BUS0	G4	VCAMA	M14	VSIM2
C1	TX_LB	G5	TESTMODE	M15	LPTE
C12	VDDK	G6	AVSS44_ALDO	M16	SIM2_SRST
C13	KCOL2	G7	GND	M2	AVSS_SPK
C14	KCOL3	G8	GND	M4	VSBST
C15	KROW3	G9	GND	M5	VSBST
C16	KROW4	H12	GPIO_9	M7	AU_VIN0_P
C2	AVSS_2G	H13	GPIO_8	M8	APC
C5	SRCLKENAI	H14	GPIO_7	N1	SPK_OUTP
C8	AVDD15_BTRF	H15	GPIO_6	N11	VUSB
C9	CMCSD1	H2	CHRLDO	N13	MCDA3
D1	AVSS_2G	H3	BATSNS	N14	MCCM0
D12	GND	H4	ISENSE	N15	MCDA1
D14	KCOL4	H8	GND	N16	SIM2_SCLK
D15	URXD1	H9	GND	N2	AVSS_SPK
N4	AVSS44_BOOST	P4	VSBST_OUT	R15	MCCK

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Pin#	Net name	Pin#	Net name	Pin#	Net name
N5	AVSS44_BOOST	P5	AVSS28_ABB	R16	VMC
N7	AU_VIN0_N	P6	AU_VIN1_P	R2	AU_HPL
N8	AUXIN4	P7	AU_VIN1_N	R3	AU_HSP
P10	USB11_DM	P8	VCORE	R4	AU_HSN
P11	USB11_DP	P9	VRTC	R5	VA
P12	SIM1_SCLK	R1	AU_HPR	R7	AVSS28_ABB
P13	MCDA2	R10	VIBR	R9	VBAT_DIGITAL
P15	MCDA0	R12	SIM1_SRST		
P2	AVDD_SPK	R13	VSIM1		

2.1.3 Detailed Pin Description

Table 2. Acronym for pin types

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 3. PIN function description and power domain

Pin name	Type	Description	Power domain
System			
RESETB	DIO	System reset	DVDD18_EMI
SRCLKENAI	DIO	26MHz clock request by external devices	VRF
EINT	DIO	External Interrupt	VRF
GPIO_0	DIO	General purpose input /output 0	DVDD28
GPIO_1	DIO	General purpose input /output 1	DVDD28
GPIO_2	DIO	General purpose input /output 2	DVDD28
GPIO_3	DIO	General purpose input /output 3	DVDD28
GPIO_4	DIO	General purpose input /output 4	DVDD28
GPIO_5	DIO	General purpose input /output 5	DVDD28
GPIO_6	DIO	General purpose input /output 6	DVDD28
GPIO_7	DIO	General purpose input /output 7	DVDD28
GPIO_8	DIO	General purpose input /output 8	DVDD28
GPIO_9	DIO	General purpose input /output 9	DVDD28

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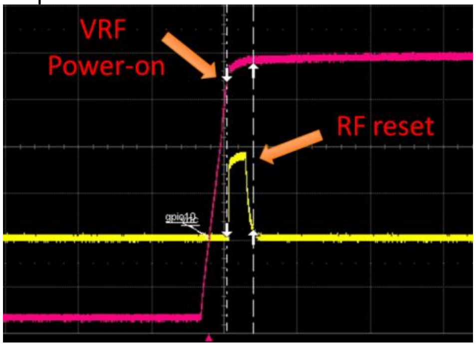
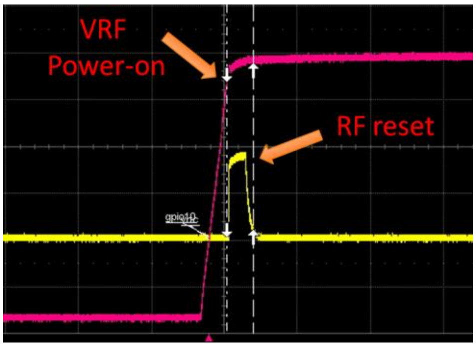
Pin name	Type	Description	Power domain
GPIO_10	DIO	General purpose input /output 10, with analog output function, please be notified that this GPIO may temporarily output high signal after VRF power-on then output low once RF circuit reset done  	VRF
GPIO_11	DIO	General purpose input /output 11, with analog output function, please be notified that this GPIO temporarily output high signal after VRF power-on then output low once RF circuit reset done  	VRF
RF control circuitro			
BPI_BUS0	DIO	RF hard-wire control bus bit 0	DVDD28
BPI_BUS1	DIO	RF hard-wire control bus bit 1	DVDD28
BPI_BUS2	DIO	RF hard-wire control bus bit 2	DVDD28
UART interface			
URXD1	DIO	UART1 receive data	DVDD28
UTXD1	DIO	UART1 transmit data	DVDD28
Keypad interface			
KCOL0	DIO	Keypad column 0	DVDD28
KCOL1	DIO	Keypad column 1	DVDD28
KCOL2	DIO	Keypad column 2	DVDD28
KCOL3	DIO	Keypad column 3	DVDD28
KCOL4	DIO	Keypad column 4	DVDD28
KROW0	DIO	Keypad row 0	DVDD28
KROW1	DIO	Keypad row 1	DVDD28

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Pin name	Type	Description	Power domain
KROW2	DIO	Keypad row 2	DVDD28
KROW3	DIO	Keypad row 3	DVDD28
KROW4	DIO	Keypad row 4	DVDD28
Camera interface			
CMRST	DIO	CMOS sensor reset signal output	DVDD28
CMPDN	DIO	CMOS sensor power down control	DVDD28
CMCSD0	DIO	CMOS sensor data input 0	DVDD28
CMCSD1	DIO	CMOS sensor data input 1	DVDD28
CMMCLK	DIO	CMOS sensor pixel clock input	DVDD28
CMCSK	DIO	CMOS sensor pixel clock output	DVDD28
MS/SD card interface			
MCDA0	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCDA1	DIO	SD serial data IO 1/memory stick serial data IO	DVDD33_MSDC
MCDA2	DIO	SD serial data IO 2/memory stick serial data IO	DVDD33_MSDC
MCDA3	DIO	SD serial data IO 3/memory stick serial data IO	DVDD33_MSDC
MCCK	DIO	SD serial clock/memory stick serial clock	DVDD33_MSDC
MCCM0	DIO	SD command output/memory stick bus state output	DVDD33_MSDC
SIM card interface			
SIM1_SIO	DIO	SIM1 data input/outputs	VSIM1
SIM1_SRST	DIO	SIM1 card reset output	VSIM1
SIM1_SCLK	DIO	SIM1 card clock output	VSIM1
SIM2_SIO	DIO	SIM2 data input/outputs	VSIM2
SIM2_SRST	DIO	SIM2 card reset output	VSIM2
SIM2_SCLK	DIO	SIM2 card clock output	VSIM2
I2C interface			
SCL28	DIO	I2C clock 2.8v power domain	DVDD28
SDA28	DIO	I2C data 2.8v power domain	DVDD28
LCD interface			
LSRSTB	DIO	Serial display interface reset signal	DVDD18_EMI
LSCE_B	DIO	Serial display interface chip select output	DVDD18_EMI
LSCK	DIO	Serial display interface clock	DVDD18_EMI
LSDA	DIO	Serial display interface data	DVDD18_EMI
LSA0	DIO	Serial display interface address	DVDD18_EMI
LPTE	DIO	Serial display tearing signal	DVDD18_EMI
FM			
FM_ANT_P	AI	FM input from antenna	VCAMA
Bluetooth			
BT_LNA	AIO	Bluetooth RF single-ended input	DVDD28

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Pin name	Type	Description	Power domain
2G RF			
RXHB	AI	RF input for highband Rx (DCS/PCS)	VRF
RXLB	AI	RF input for lowband Rx (GSM900/GSM850)	VRF
TX_HB	AO	RF output for highband Tx (DCS/PCS)	VRF
TX_LB	AO	RF output pin for lowband Tx (GSM900/GSM850)	VRF
FREF	AO	DCXO reference clock output	VRF
XTAL1	AIO	Input 1 for DCXO crystal	VRF
XTAL2	AIO	Input 2 for DCXO crystal	VRF
EXT_CLK_SEL	AIO	DCXO mode selection	VRF
USB			
USB11_DM	AIO	D- data input/output	-
USB11_DP	AIO	D+ data input/output	-
Analog baseband			
AU_HPR	AIO	Audio head phone output (R channel)	AVDD28_ABB
AU_HPL	AIO	Audio head phone output (L channel)	AVDD28_ABB
AU_HSP	AIO	Voice handset output (positive)	AVDD28_ABB
AU_HSN	AIO	Voice handset output (negative)	AVDD28_ABB
AU_VIN0_P	AIO	Microphone 0 input (positive)	AVDD28_ABB
AU_VIN0_N	AIO	Microphone 0 input (negative)	AVDD28_ABB
AU_VIN1_P	AIO	Microphone 1 input (positive)	AVDD28_ABB
AU_VIN1_N	AIO	Microphone 1 input (negative)	AVDD28_ABB
AUX_IN4	AIO	Auxiliary ADC input	AVDD28_ABB
SPK_OUTP	AIO	Speaker positive output	VBAT_SPK
SPK_OUTN	AIO	Speaker negative output	VBAT_SPK
APC	AIO	Automatic power control DAC output	AVDD28_ABB
AU_MICBIAS0	AIO	Microphone bias source 0	AVDD28_ABB
ACCDET	AIO	Accessory detection	AVDD28_ABB
Power management unit			
VA	AIO	LDO output for ABB - VA	VBAT_ANALOG
VCAMA	AIO	LDO output for sensor – VCAMA	VBAT_VA
VIBR	AIO	LDO output for vibrator - VIBR	VBAT_DIGITAL
VIO18	AIO	LDO output for 1.8V power - VIO18	VBAT_DIGITAL
VIO28	AIO	LDO output for 2.8V power - VIO28	VBAT_DIGITAL
VMC	AIO	LDO output for memory card - VMC	VBAT_DIGITAL
VSF	AIO	LDO output - VSF	VBAT_DIGITAL
VRF	AIO	LDO output for GSMRF - VRF	VBAT_VA
VRTC	AIO	LDO output for RTC - VRTC	VBAT_DIGITAL
VSIM1	AIO	LDO output for 1st SIM - VSIM	VBAT_DIGITAL
VSIM2	AIO	LDO output for 2nd SIM - VSIM2	VBAT_DIGITAL
VUSB	AIO	LDO output for USB - VUSB	VBAT_DIGITAL

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Pin name	Type	Description	Power domain
VCORE	AIO	LDO output for core circuit - Vcore	VBAT_DIGITAL
VREF	AIO	Band gap reference	BATSNS
VCDT	AIO	Charger-In level sense pin	BATSNS
DRV	AIO	IDAC current output open-drain pin	BATSNS
BATON	AIO	Battery Pack, NTC connected pin	BATSNS
ISENSE	AIO	Top node of current sensing 0.2ohm Rsense resistor	BATSNS
CHRLDO	AIO	2.8V shunt-regulator output	BATSNS
BATDET	AIO	Battery detection pin	BATSNS
ISINK0	AIO	Backlight driver channel 0	VBAT_VA
KPLED	AIO	Keypad led driver	VBAT_VA
VSBST_OUT	AIO	Audio boost output	VSBST
TESTMODE	AIO	Test mode	BATSNS
PWRKEY	AIO	PWR key	BATSNS
AVDD25_V2P5	AIO	Reference voltage for ABT	-
Analog power			
VSBST	P	VBAT input for audio boost	
AVDD15_BTRF	P	BTRF power input	-
VBAT_DIGITAL	P	Digital LDOs used battery voltage input	-
VBAT_VA	P	Analog LDOs used battery voltage input	-
AVDD_SPK	P	Input for loud speaker driver	-
BATSNS	P	Battery node of battery pack	-
AVDD15_BTRF	P	BTRF power input	-
Analog ground			
AVSS28_ABB	G	ABB 2.8V ground	-
AVSS_BT	G	BT ground	-
AVSS_2G	G	2G RF ground	-
AVSS_FM	G	FM ground	-
AVSS44_PMU	G	PMU ground	-
AVSS44_ALDO	G	ALDO ground	-
AVSS44_DLDO	G	DLDO ground	-
AVSS_SPK	G	SPK ground	-
AGND	G	GND for VREF	-
AVSS44_BOOST	G	Audio boost GND	-
Digital power			
VDDK	P	Core power	-
Digital ground			
GND	G	Ground	-

Table 4. Acronym for state of pins

Abbreviation	Description

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Abbreviation	Description
I	Input
LO	Low output
HO	High output
LO	Low output
PU	Pull-up
PD	Pull-down
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 5. State of pins

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
System						
RESETB	HO	1	-	DIOH3/DIOL3	No need	IO Type 3
SRCLKENAI	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
EINT	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_0	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_1	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_3	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_4	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_5	LO	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_6	LO	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_7	LO	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_8	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_9	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_10	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_11	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
RF control circuitry						

[1] The column "State" of "Reset" shows the pin state during reset. (Input, High Output, Low Output, etc)

[2] The column "Aux" for "Reset" means the default aux function number, shown in the table "Pin Multiplexing, Capability and Settings".

[3] The column "PU/PD" for "Reset" means if there is internal pull-up or pull-down when the pin is input in the reset state.

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Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
BPI_BUS0	LO	1	PD	DIOH2/DIOL2	No need	IO Type 2
BPI_BUS1	I	1	PD	DIOH2/DIOL2	No need	IO Type 2
BPI_BUS2	I	1	PD	DIOH2/DIOL2	No need	IO Type 2
UART interface						
URXD1	I	1	PU	DIOH3/DIOL3	No need	IO Type 3
UTXD1	HO	1	PU	DIOH2/DIOL2	No need	IO Type 2
Keypad Interface						
KCOL0	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL1	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL2	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL3	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL4	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KROW0	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW1	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW2	I	0	PD	DIOH6/DIOL6	No need	IO Type 6
KROW3	I	0	PD	DIOH6/DIOL6	No need	IO Type 6
KROW4	I	0	PD	DIOH6/DIOL6	No need	IO Type 6
Camera interface						
CMRST	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
CMPDN	HO	0	-	DIOH3/DIOL3	No need	IO Type 3
CMCSD0	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
CMCSD1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
CMMCLK	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
CMCSK	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
MS/SD card interface						
MCDA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA2	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA3	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCCK	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
MCCM0	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
SIM card interface						
SIM1_SIO	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM1_SRST	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM1_SCLK	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SIO	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SRST	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SCLK	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
I2C interface						
SCL28	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
SDA28	I	0	PD	DIOH2/DIOL2	No need	IO Type 2

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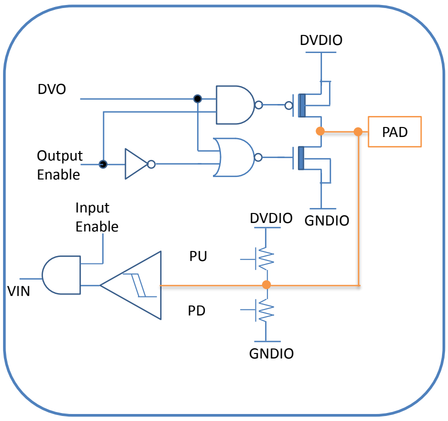
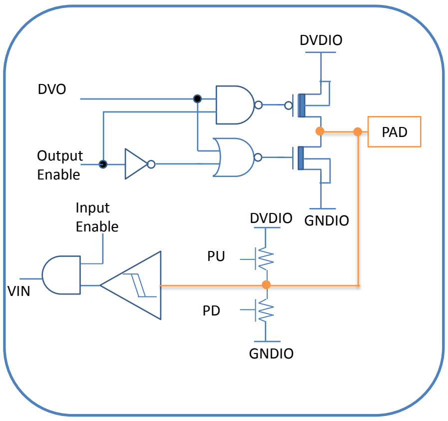
Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
LCD interface						
LSRSTB	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSCE_B	HO	1	-	DIOH3/DIOL3	No need	IO Type 3
LSCK	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSDA	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LPTE	I	0	PD	DIOH3/DIOL3	No need	IO Type 3



IO type1



IO type2

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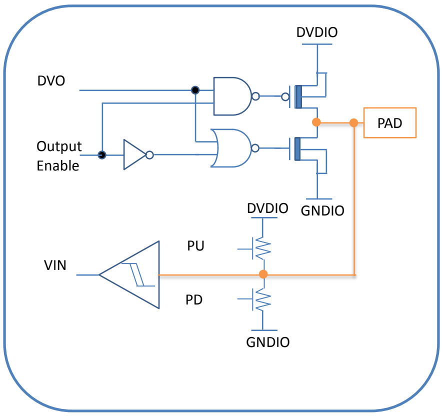
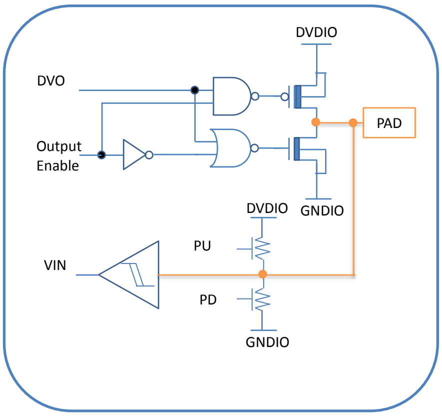


IO type3



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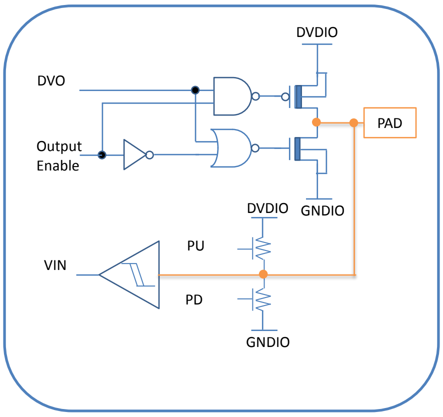
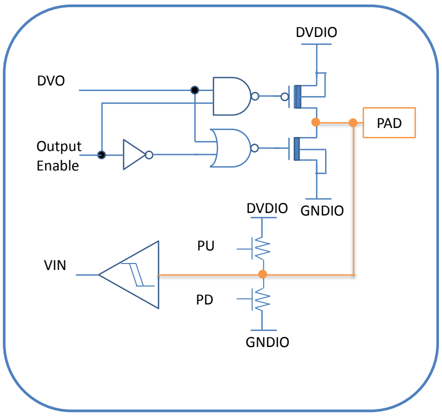


IO type5



IO type6

Figure 4. IO types in state of pins

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2.1.4 Pin Multiplexing, Capability and Settings

Table 6. Acronym for pull-up and pull-down types

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-down

Table 7. Capability of PU/PD, driving and Schmitt trigger

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
GPIO_0	0	GPIO0	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT0	I	CU, CD	4, 8, 12, 16mA	0
	2	XP	AIO	-	4, 8, 12, 16mA	0
	3	U3RXD	I	CU, CD	4, 8, 12, 16mA	0
	4	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	5	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	6	EDIDO	O	CU, CD	4, 8, 12, 16mA	0
	7	JTDI	I	PU	4, 8, 12, 16mA	0
	8	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
GPIO_1	0	GPIO1	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT1	I	CU, CD	4, 8, 12, 16mA	0
	2	XM	AIO	-	4, 8, 12, 16mA	0
	3	U3TXD	O	CU, CD	4, 8, 12, 16mA	0
	4	U1CTS	I	CU, CD	4, 8, 12, 16mA	0
	5	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
	6	EDIDI	I	CU, CD	4, 8, 12, 16mA	0
	7	JTMS	I	PU	4, 8, 12, 16mA	0
	8	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
GPIO_2	0	GPIO2	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT2	O	CU, CD	4, 8, 12, 16mA	0
	2	YP	AIO	-	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	3	GPSFSYNC	O	CU, CD	4, 8, 12, 16mA	0
	4	PWM0	O	CU, CD	4, 8, 12, 16mA	0
	5	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	6	EDIWS	O	CU, CD	4, 8, 12, 16mA	0
	7	JTRST_B	I	PD	4, 8, 12, 16mA	0
	8	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
GPIO_3	0	GPIO3	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	2	YM	AIO	-	4, 8, 12, 16mA	0
	4	PWM1	O	CU, CD	4, 8, 12, 16mA	0
	5	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	6	EDICK	O	CU, CD	4, 8, 12, 16mA	0
	7	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	8	BTJTDO	O	CU, CD	4, 8, 12, 16mA	0
	9	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
GPIO_4	0	GPIO4	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT3	I	CU, CD	4, 8, 12, 16mA	0
	4	U1RTS	O	CU, CD	4, 8, 12, 16mA	0
GPIO_5	0	GPIO5	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT4	I	CU, CD	4, 8, 12, 16mA	0
	3	BPI_BUS3	O	CU, CD	4, 8, 12, 16mA	0
GPIO_6	0	GPIO6	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT5	I	CU, CD	4, 8, 12, 16mA	0
	2	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	3	BPI_BUS4	O	CU, CD	4, 8, 12, 16mA	0
GPIO_7	0	GPIO7	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT6	I	CU, CD	4, 8, 12, 16mA	0
	3	BPI_BUS5	O	CU, CD	4, 8, 12, 16mA	0
GPIO_8	0	GPIO8	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT7	I	CU, CD	4, 8, 12, 16mA	0
	2	SCL	IO	CU, CD	4, 8, 12, 16mA	0
GPIO_9	0	GPIO9	IO	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	EINT8	I	CU, CD	4, 8, 12, 16mA	0
	2	SDA	IO	CU, CD	4, 8, 12, 16mA	0
URXD1	0	GPIO10	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1RXD	I	PU	4, 8, 12, 16mA	0
	2	CMRST	O	CU, CD	4, 8, 12, 16mA	0
	3	EINT9	I	CU, CD	4, 8, 12, 16mA	0
	4	MCINS	I	CU, CD	4, 8, 12, 16mA	0
UTXD1	0	GPIO11	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1TXD	O	CU, CD	4, 8, 12, 16mA	0
	2	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
	3	EINT10	I	CU, CD	4, 8, 12, 16mA	0
KCOL4	0	GPIO12	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL4	IO	-	4, 8, 12, 16mA	0
	2	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	3	EDIDI	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	5	JTDI	I	PU	4, 8, 12, 16mA	0
	6	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
KCOL3	0	GPIO13	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL3	IO	-	4, 8, 12, 16mA	0
	2	EINT11	I	CU, CD	4, 8, 12, 16mA	0
	3	PWM0	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	5	JTMS	I	PU	4, 8, 12, 16mA	0
	6	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
KCOL2	0	GPIO14	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL2	IO	-	4, 8, 12, 16mA	0
	2	EINT12	I	CU, CD	4, 8, 12, 16mA	0
	3	U1RTS	I	CU, CD	4, 8, 12, 16mA	0
KCOL1	0	GPIO15	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL1	IO	-	4, 8, 12, 16mA	0
	2	GPSFSYNC	O	CU, CD	4, 8, 12, 16mA	0
	3	U1CTS	I	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	PU	4, 8, 12, 16mA	0
	6	BTJTCK	I	CU, CD	4, 8, 12, 16mA	0
KCOL0	0	GPIO16	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL0	IO	-	4, 8, 12, 16mA	0
KROW4	0	GPIO17	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW4	IO	-	4, 8, 12, 16mA	0
	2	U2TXD	O	CU, CD	4, 8, 12, 16mA	0
	3	EDICK	O	CU, CD	4, 8, 12, 16mA	0
KROW3	0	GPIO18	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW3	IO	-	4, 8, 12, 16mA	0
	2	EINT13	I	CU, CD	4, 8, 12, 16mA	0
	3	CLKO0	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRST_B	I	PD	4, 8, 12, 16mA	0
	6	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
KROW2	0	GPIO19	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW2	IO	-	4, 8, 12, 16mA	0
	2	PWM1	O	CU, CD	4, 8, 12, 16mA	0
	3	EDIWS	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
	5	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	6	BTJTDO	O	CU, CD	4, 8, 12, 16mA	0
KROW1	0	GPIO20	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW1	IO	-	4, 8, 12, 16mA	0
	2	EINT14	I	CU, CD	4, 8, 12, 16mA	0
	3	EDIDO	O	CU, CD	4, 8, 12, 16mA	0
	4	BTPRI	IO	CU, CD	4, 8, 12, 16mA	0
	5	JTRCK	O	CU, CD	4, 8, 12, 16mA	0
	6	BTDBGACKN	O	CU, CD	4, 8, 12, 16mA	0
KROW0	0	GPIO21	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW0	IO	-	4, 8, 12, 16mA	0
	5	MCINS	I	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	6	BTDBGIN	I	CU, CD	4, 8, 12, 16mA	0
BPI_BUS2	0	GPIO22	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS2	O	CU, CD	4, 8, 12, 16mA	0
BPI_BUS1	0	GPIO23	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS1	O	CU, CD	4, 8, 12, 16mA	0
BPI_BUS0	0	GPIO24	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS0	IO	CU, CD	4, 8, 12, 16mA	0
CMRST	0	GPIO25	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMRST	O	CU, CD	4, 8, 12, 16mA	0
	2	LSRSTB	O	CU, CD	4, 8, 12, 16mA	0
	3	CLKO1	O	CU, CD	4, 8, 12, 16mA	0
	4	EINT15	I	CU, CD	4, 8, 12, 16mA	0
	5	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	6	JTDI	I	PU	4, 8, 12, 16mA	0
CMPDN	0	GPIO26	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
	2	LSCK1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAICLK	O	CU, CD	4, 8, 12, 16mA	0
	4	SPICS	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	6	JTMS	I	PU	4, 8, 12, 16mA	0
CMCSD0	0	GPIO27	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCE_B1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
	4	SPISCK	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	6	JTCK	I	PU	4, 8, 12, 16mA	0
	8	MC2CM0	O	-	4, 8, 12, 16mA	0
CMCSD1	0	GPIO28	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDA1	IO	CU, CD	4, 8, 12, 16mA	0
	3	DAIPCMOUT	O	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	SPIMOSI	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	6	JTRST_B	I	PD	4, 8, 12, 16mA	0
	8	MC2CK	O	-	4, 8, 12, 16mA	0
CMMCLK	0	GPIO29	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
	2	LSA0DA1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAISYNC	O	CU, CD	4, 8, 12, 16mA	0
	4	SPIMISO	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
	6	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	8	MC2DA0	IO	-	4, 8, 12, 16mA	0
CMCSK	0	GPIO30	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	2	LPTE	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	4	EINT16	I	CU, CD	4, 8, 12, 16mA	0
	6	JTRCK	O	CU, CD	4, 8, 12, 16mA	0
MCCK	0	GPIO31	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCK	O	-	4, 8, 12, 16mA	0
	4	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
MCCM0	0	GPIO32	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCM0	IO	-	4, 8, 12, 16mA	0
	4	U2TXD	O	CU, CD	4, 8, 12, 16mA	0
MCDA0	0	GPIO33	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	-	4, 8, 12, 16mA	0
	4	DAISYNC	O	CU, CD	4, 8, 12, 16mA	0
MCDA1	0	GPIO34	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA1	IO	-	4, 8, 12, 16mA	0
	2	EINT17	I	CU, CD	4, 8, 12, 16mA	0
	4	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
MCDA2	0	GPIO35	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA2	IO	-	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	2	EINT18	I	CU, CD	4, 8, 12, 16mA	0
	4	DAICLK	O	CU, CD	4, 8, 12, 16mA	0
MCDA3	0	GPIO36	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA3	IO	-	4, 8, 12, 16mA	0
	2	EINT19	I	CU, CD	4, 8, 12, 16mA	0
	3	CLKO2	O	CU, CD	4, 8, 12, 16mA	0
	4	DAIPCMOUT	O	CU, CD	4, 8, 12, 16mA	0
SIM1_SIO	0	GPIO37	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SIO	IO	-	2, 4, 6, 8mA	0
SIM1_SRST	0	GPIO38	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SRST	IO	-	2, 4, 6, 8mA	0
SIM1_SCLK	0	GPIO39	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SCLK	IO	-	2, 4, 6, 8mA	0
SIM2_SIO	0	GPIO40	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SIO	IO	-	2, 4, 6, 8mA	0
	3	U2RTS	O	CU, CD	2, 4, 6, 8mA	0
SIM2_SRST	0	GPIO41	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SRST	IO	-	2, 4, 6, 8mA	0
	2	CLKO3	O	CU, CD	2, 4, 6, 8mA	0
	3	U2CTS	I	CU, CD	2, 4, 6, 8mA	0
SIM2_SCLK	0	GPIO42	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SCLK	IO	-	2, 4, 6, 8mA	0
	2	LSCE1_B1	O	CU, CD	2, 4, 6, 8mA	0
SCL	0	GPIO43	IO	CU, CD	4, 8, 12, 16mA	0
	1	SCL	IO	CU, CD	4, 8, 12, 16mA	0
SDA	0	GPIO44	IO	CU, CD	4, 8, 12, 16mA	0
	1	SDA	IO	CU, CD	4, 8, 12, 16mA	0
LSRSTB	0	GPIO45	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSRSTB	O	CU, CD	4, 8, 12, 16mA	0
	3	CMRST	O	CU, CD	4, 8, 12, 16mA	0
LSCE_B0	0	GPIO46	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSCE_B0	O	CU, CD	4, 8, 12, 16mA	0
	2	EINT20	I	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	3	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	4	CLKO4	O	CU, CD	4, 8, 12, 16mA	0
LSCK0	0	GPIO47	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSCK0	O	CU, CD	4, 8, 12, 16mA	0
	3	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
LSDA0	0	GPIO48	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSDA0	IO	-	4, 8, 12, 16mA	0
	2	EINT21	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	4	WIFITOBT	I	CU, CD	4, 8, 12, 16mA	0
LSA0	0	GPIO49	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSA0DA0	O	-	4, 8, 12, 16mA	0
	2	LSCE1_B0	O	CU, CD	4, 8, 12, 16mA	0
	3	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
LPTE	0	GPIO50	IO	CU, CD	4, 8, 12, 16mA	0
	1	LPTE	I	CU, CD	4, 8, 12, 16mA	0
	2	EINT22	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	4	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	6	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	9	CLKO5	O	CU, CD	4, 8, 12, 16mA	0
RESETB	0	GPIO51	IO	CU, CD	4, 8, 12, 16mA	0
	1	RESETB	IO	CU, CD	4, 8, 12, 16mA	0
EINT	0	AGPI52	I	CU, CD	8mA	0
	2	EINT23	I	CU, CD	8mA	0
SRCLKENAI	0	AGPI53	I	CU, CD	8mA	0
	1	SRCLKENAI	I	CU, CD	8mA	0
	2	EINT24	I	-	8mA	0
GPIO_10	0	AGPIO54	IO	CU, CD	8mA	0
GPIO_11	0	AGPIO55	IO	CU, CD	8mA	0

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2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 8. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	-0.3	+4.4	V
VBAT_VA	Analog used battery voltage input	-0.3	+4.4	V
AVDD_SPK	VBAT input for loud speaker driver	-0.3	+5.5	V
VSBST	Boost used battery voltage input	-0.3	+4.4	V
VDDK	1.3v core power	-0.3	+1.43	V

Table 9. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.08	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.08	V
VIN3	Digital input voltage for IO Type 3	-0.3	3.63	V
VIN4	Digital input voltage for IO Type 4	-0.3	3.08	V
VIN5	Digital input voltage for IO Type 5	-0.3	3.08	V
VIN6	Digital input voltage for IO Type 6	-0.3	3.08	V
VIN7	Digital input voltage for IO Type 7	-0.3	3.63	V

Table 10. Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	^{o}C

2.2.2 Recommended Operating Conditions

Table 11. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	3.4	3.8	4.2	V
VBAT_VA	Analog used battery voltage input	3.4	3.8	4.2	V
AVDD_SPK	VBAT input for loud speaker driver	3.4	3.8	4.2	V
VSBST	Boost used battery voltage input	3.4	3.8	4.2	V
VDDK	1.2v core power	1.17	1.3	1.43	V

Table 12. Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ.	Max.	Unit

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V
VIN4	Digital input voltage for IO Type 4	-0.3	-	DVDIO+0.3	V
VIN5	Digital input voltage for IO Type 5	-0.3	-	DVDIO+0.3	V
VIN6	Digital input voltage for IO Type 6	-0.3	-	DVDIO+0.3	V
VIN7	Digital input voltage for IO Type 7	-0.3	-	DVDIO+0.3	V

Table 13. Recommended operating conditions for operating temperature

Symbol or pin name	Description	Min.	Typ	Max.	Unit
Tc	Operating temperature	-20	-	85	°C

2.2.3 Electrical Characteristics under Recommended Operating Conditions

Table 14. Electrical characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
DIIL1	Digital low input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-12.5	-	22.5	
DIOH1	Digital high output current for IO Type 1	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL1	Digital low output current for IO Type 1	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DVOH1	Digital output high voltage for IO Type 1	DVDIO = 2.8V	2.38			V
DVOL1	Digital output low voltage for IO Type 1	DVDIO = 2.8V			0.42	V
DIIH2	Digital high input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-9.3	-	11.4	
DIOH2	Digital high output current for IO Type 2	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digital output high voltage for IO Type 2	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL2	Digital output low voltage for IO Type 2	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH3	Digital high input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-0.8	-	35	
DIIL3	Digital low input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-35	-	0.8	

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-9.3	-	11.4	
DIOH3	Digital high output current for IO Type 3	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL3	Digital low output current for IO Type 3	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU3	Digital I/O pull-up resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	DVDIO = 1.8V	10	47	100	kΩ
		DVDIO = 2.8V	10	47	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL3	Digital output low voltage for IO Type 3	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH4	Digital high input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	6.1	-	82.5	
DIIL4	Digital low input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-12.5	-	22.5	
DIOH4	Digital high output current for IO Type 4	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL4	Digital low output current for IO Type 4	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU4	Digital I/O pull-up resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DRPD4	Digital I/O pull-down resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPU4 1200K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1200	-	-	kΩ
DRPD4 1200K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1200	-	-	kΩ
DVOH4	Digital output high voltage for IO Type 4	DVDIO = 2.8V	2.38			V
DVOL4	Digital output low voltage for IO Type 4	DVDIO = 2.8V			0.42	V
DIIH5	Digital high input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	6.1	-	82.5	
DIIL5	Digital low input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-12.5	-	22.5	
DIOH5	Digital high output current for IO Type 5	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL5	Digital low output current for IO Type 5	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU5	Digital I/O pull-up resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPD5	Digital I/O pull-down resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPU5 1K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	-	kΩ
DRPD5 1K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	-	kΩ
DVOH5	Digital output high voltage for IO Type 5	DVDIO = 2.8V	2.38			V

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DVOL5	Digital output low voltage for IO Type 5	DVDIO = 2.8V			0.42	V
DIIH6	Digital high input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-0.8	-	35	
DIIL6	Digital low input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-9.3	-	11.4	
DIOH6	Digital high output current for IO Type 6	DVOH > 2.38V, DVDIO = 2.8V	-8	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-6	-	-	mA
DIOL6	Digital low output current for IO Type 6	DVOL < 0.42V, DVDIO = 2.8V	-	-	8	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	6	mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DRPU6	Digital I/O pull-up resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD6	Digital I/O pull-down resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH6	Digital output high voltage for IO Type 6	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL6	Digital output low voltage for IO Type 6	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH7	Digital high input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN7<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-0.8	-	35	
DIIL7	Digital low input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIOH7	Digital high output current for IO Type 7	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL7	Digital low output current for IO Type 7	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU7	Digital I/O pull-up resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD7	Digital I/O pull-down resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH7	Digital output high voltage for IO Type 7	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL7	Digital output low voltage for IO Type 7	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

2.3 System Configuration

2.3.1 Strapping Resistors

Table 15. Strapping table

Pin name	Description	Trapping condition
LSA0	Pull-up with 10K resister(Default internal pull-down with 47K resister)	Power-on reset
BPI_BUS1	Pull-up with 10K resister (Default internal pull-down with 75K resister)	Power-on reset
BPI_BUS2	Pull-up with 10K resister (Default internal pull-down with 75K resister)	Power-on reset

2.3.2 Mode Selection

Table 16. Mode selection of chip

Pin name	Description
EXT_CLK_SEL	GND: Uses DCXO as 26M clock source VRF: Uses external clock as 26M clock source
LSA0	GND: Uses 1.8V serial flash device DVDD18_EMI: Uses 3.3V serial flash device
KCOL0	GND: Boots ROM to enter USB download mode DVDD28: Normal boot-up mode
{BPI_BUS1,BPI_BUS2}	{GND, GND}: No JTAG {GND, DVDD28}: JTAG at keypad pins

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	{DVDD28, GND}: JTAG at GPIO pins {DVDD28, DVDD28}: JTAG at camera pins

2.4 Power-on Sequence and Protection Logic

MT6261D provides 32K crystal removal feature. The XOSC32_ENB state tells if MT6261D provides this feature or not. VRF will be turned on at the same time with VRTC when XOSC32_ENB = 1. The power-on/off sequence controlled by “Control” and “Reset Generator” is shown as the figure below.

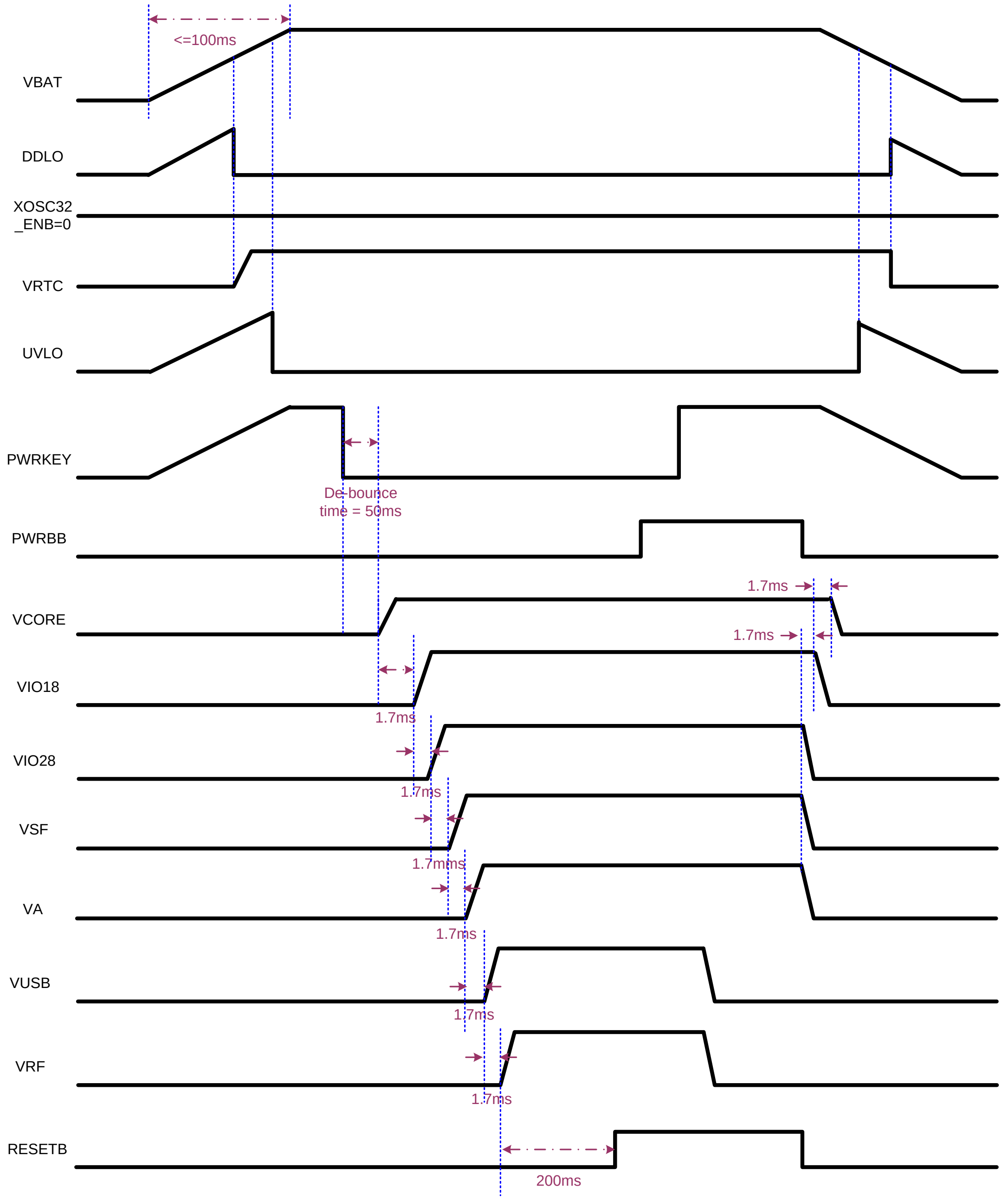

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Figure 5. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 0

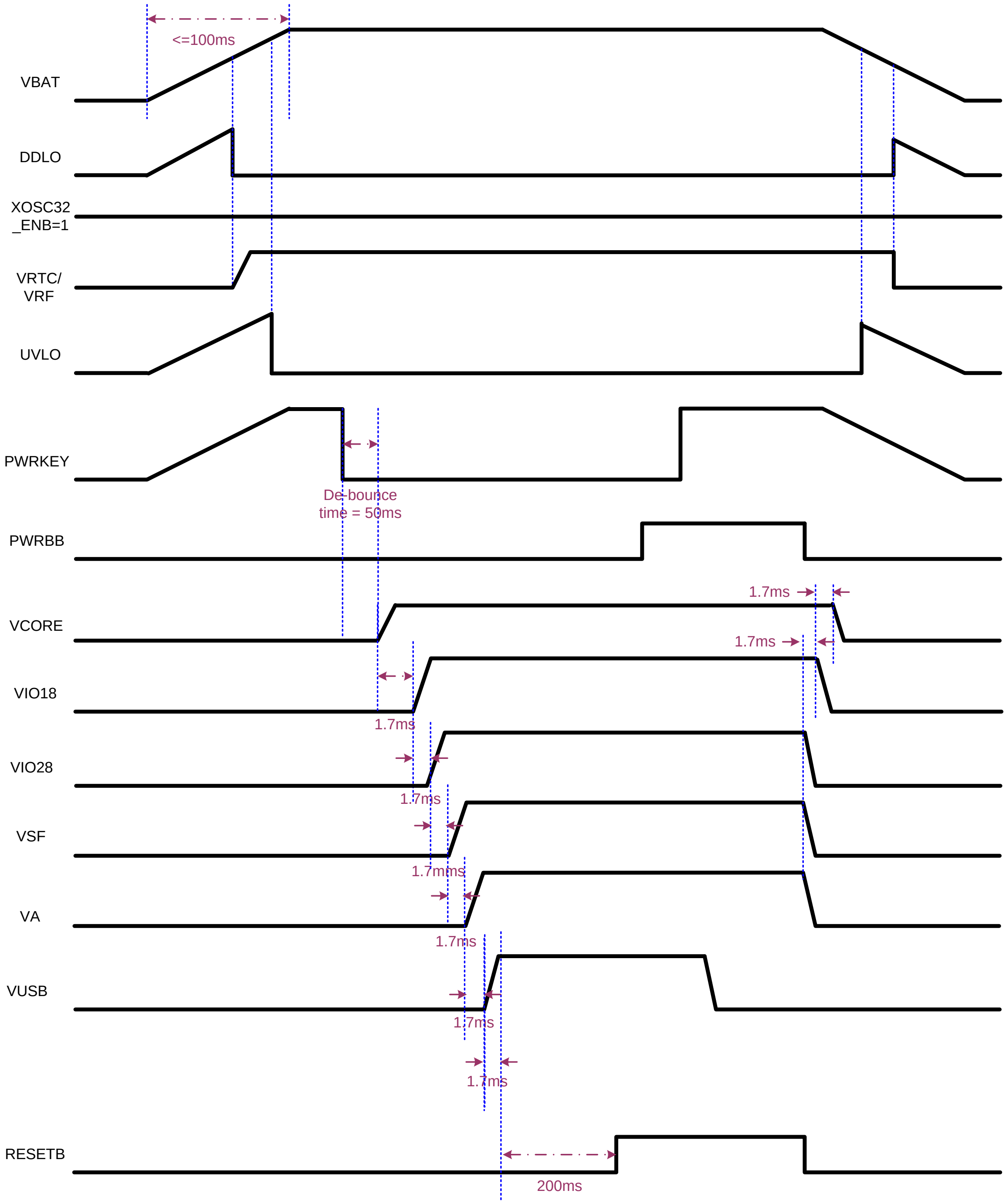

Figure 6. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 1

Note that each of the above figures only shows one power-on/off condition when XOSC32_ENB = 0 or XOSC32_ENB = 1. MT6261D handles the power-on and off of the handset. The following three methods can switch on the handset (when leaving UVLO): XOSC32_ENB = 0

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1. Push PWRKEY (Pull the PWRKEY pin to the low level.)

   Pulling PWRKEY low is the typical way to turn on the handset. The turn-on sequence is VCORE → VIO18 → VIO28 → VSF → VA → VUSB → VRF.

   The supplies for the baseband are ready, and the system reset ends at the moment when the above LDOs are fully turned on to ensure correct timing and function. After that, the baseband will send the PWRBB signal back to the PMU for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMU receives PWRBB from the baseband.

2. RTC module generates PWRBB to wake up the system.

   If the RTC module is scheduled to wake up the handset at a certain time, the PWRBB signal will be directly sent to the PMU. In this case, PWRBB will become high at specific moment and allow the PMU to be powered on as the sequence described above. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage is within the valid range.)

   The charger plug-in will also turn on the handset if the charger is valid (no OVP takes place). However, if the battery voltage is too low to power on the handset (UVLO state), the system will not be turned on by any of the three methods. In this case, the charger will charge the battery first and the handset will be powered on automatically as long as the battery voltage is high enough.

Under-voltage lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below the 3.2V threshold. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures a smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once the PMU enters the UVLO state, it will draw low quiescent current. The RTC LDO will still be working until the DDLO disables it.

Deep discharge lockout (DDLO)

The PMU will enter the deep discharge lockout (DDLO) state when the battery voltage drops below 2.5V. In this state, the VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or damage to the cells.

Reset

The PMU contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter which uses the clock from internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

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Over-temperature protection

If the die temperature of PMU exceeds 150°C, the PMU will automatically disable all the LDOs except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the LDOs.

2.5 Analog Baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS baseband signal processing:

1. RF control: DAC for automatic power control (APC) is included, and its output is provided to external RF power amplifier respectively.

2. Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring

3. Audio mixed-signal block: Provides complete analog voice signal processing including microphone amplification, A/D conversion, D/A conversion, earphone driver, etc. Dedicated stereo D/A conversion and amplification for audio signals are also included.

4. Clock generation: Includes a clock squarer for shaping the system clock, and PLL providing clock signals to DSP, MCU and USB unit

2.5.1 APC-DAC

2.5.1.1 Block Description

APC-DAC is a 10-bit DAC with output buffer aiming at automatic power control. See the tables below for its analog pin assignment and functional specifications. It is an event-driven scheme for power saving purpose.

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2.5.1.2 Functional Specifications

Table 17. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Sampling rate			1.0833	MSPS
SINAD	Signal to noise and distortion ratio (10-kHz sine with 1.0V swing & 100-kHz BW)	47			dB
	99% settling time (full swing on maximal capacitance)			5	μS
	Output swing	0		AVDD	V
	Output capacitance		200	2200	pF
	Output resistance	0.47	10		KΩ
DNL	Differential nonlinearity for code 20 to 970		± 1		LSB
INL	Integral nonlinearity for code 20 to 970		± 1		LSB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 400 1		 μA μA

2.5.2 Auxiliary ADC

2.5.2.1 Block Description

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the seven auxiliary input pins. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.

2. 10-bit A/D converter: Converts the multiplexed input signal to 10-bit digital data.

Channel	Application	Input range [V]
0	BATSNS	3.2 ~ 4.2
1	ISENSE	3.2 ~ 4.2
2	VCDT	Decided by application circuit
3	BATON	0 ~ AVDD28
4	AUXIN4	0 ~ AVDD28
others	Internal use	N/A

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2.5.2.2 Functional Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Table 18. Functional specifications of auxiliary ADC

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FC	Clock rate		1.08		MHz
FS	Sampling rate @ N-Bit		1.08/(N+1)		MSPS
	Input swing	0		AVDD	V
CIN	Input capacitance Unselected channel Selected channel			 50 4	 fF pF
RIN	Input resistance Unselected channel Selected channel	 400 1			 MΩ MΩ
	Clock latency		N+1		1/FC
DNL	Differential nonlinearity		± 1		LSB
INL	Integral nonlinearity		± 1		LSB
OE	Offset error		± 10		mV
FSE	Full swing error		± 10		mV
SINAD	Signal to noise and distortion ratio (10-kHz full swing input & 1.0833-MHz clock rate)		50		dB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 280 1		 μA μA

2.5.3 Audio Mixed-Signal Blocks

2.5.3.1 Block Description

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. As shown in the figure below, it includes three parts. The first consists of stereo audio DACs and audio amplifiers for audio playback. The second part is the voice downlink path, including voice-band DACs (left channel audio DAC) and voice amplifier, which produces voice signals to earphones or other auxiliary output devices. Moreover, a ClassK amplifier is embedded to support continuous >1W output power with an on-chip boost. The last part is the voice uplink path, which is the interface between the microphone (or other auxiliary input device) input and MT6261D DSP. A set of bias voltage is provided for the external electric microphone.

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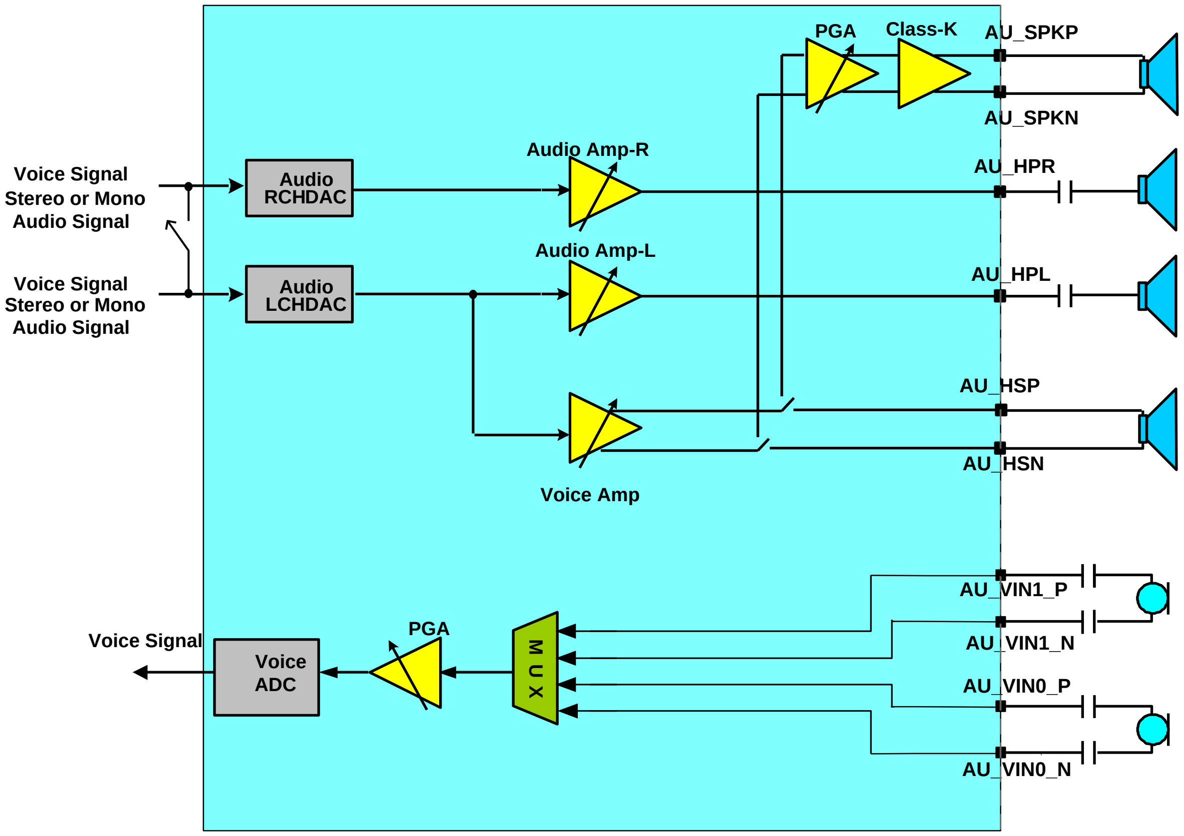

Figure 7. Block diagram of audio mixed-signal blocks

2.5.3.2 Functional Specifications

See the table below for the functional specifications of voice-band uplink/downlink blocks.

Table 19. Functional specifications of analog voice blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Sampling rate		6,500		kHz
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
VMIC	Microphone biasing voltage		1.9	2.2	V
IMIC	Current draw from microphone bias pins			2	mA
Uplink path[4]					
IDC	Current consumption for one channel		1.5		mA
SINAD	Signal to noise and distortion ratio				

[4] For uplink-path, not all gain settings of VUPG meet the specifications listed in the table, especially for several the lowest gains. The minimum gain that meets the specifications is to be determined.

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input level: -40 dbm0 Input level: 0 dbm0	29	 69		dB dB
RIN	Input impedance (differential)	13	20	27	KΩ
ICN	Idle channel noise			-67	dBm0
Downlink path					
IDC	Current consumption		4		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dBm0 Input level: 0 dBm0	 29	 69		 dB dB
RLOAD	Output resistor load (differential)	16	32		Ω
CLOAD	Output capacitor load			250	pF
ICN	Idle channel noise of transmit path			-64	dBPa
XT	Crosstalk level on transmit path			-66	dBm0

See the table below for the functional specifications of audio blocks.

Table 20. Functional specifications of analog audio blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FCK	Clock frequency		6.5		MHz
Fs	Sampling rate	32	44.1	48	kHz
AVDD	Power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
IDC	Current consumption		4		mA
PSNR	Peak signal to noise ratio		88		dB
DR	Dynamic range		88		dB
VOUT	Output swing for 0dBFS input level @ -1dB headphone gain		0.707		Vrms
$VOUT_{MAX}$	Maximum output swing		2.0		Vpp
THD	Total harmonic distortion 10mW at 64Ω load			 -70	 dB
RLOAD	Output resistor load (single-ended)	64			Ω
CLOAD	Output capacitor load			250	pF
XT	L-R channel cross talk	70			dB

2.6 Power Management Unit Blocks

The power management unit (PMU) manages the power supply of the entire chip, such as baseband, processor, memory, SIM cards, camera, vibrator, etc. The digital part of PMU is integrated into the analog part (see the figure below). PMU includes the following analog functions for signal processing:

- LDO: Regulates battery voltage to lower voltage level
- BOOST: Boosts battery voltage to target voltage for Class-AB audio amplifier

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- Keypad LED driver (KPLED) and current sink (ISINK) switches: Sink current for keypad LED and LCM module
- Start-up (STRUP): Generates power-on/off control sequence of start-up circuits
- Pulse charger (PCHR): Controls battery charging

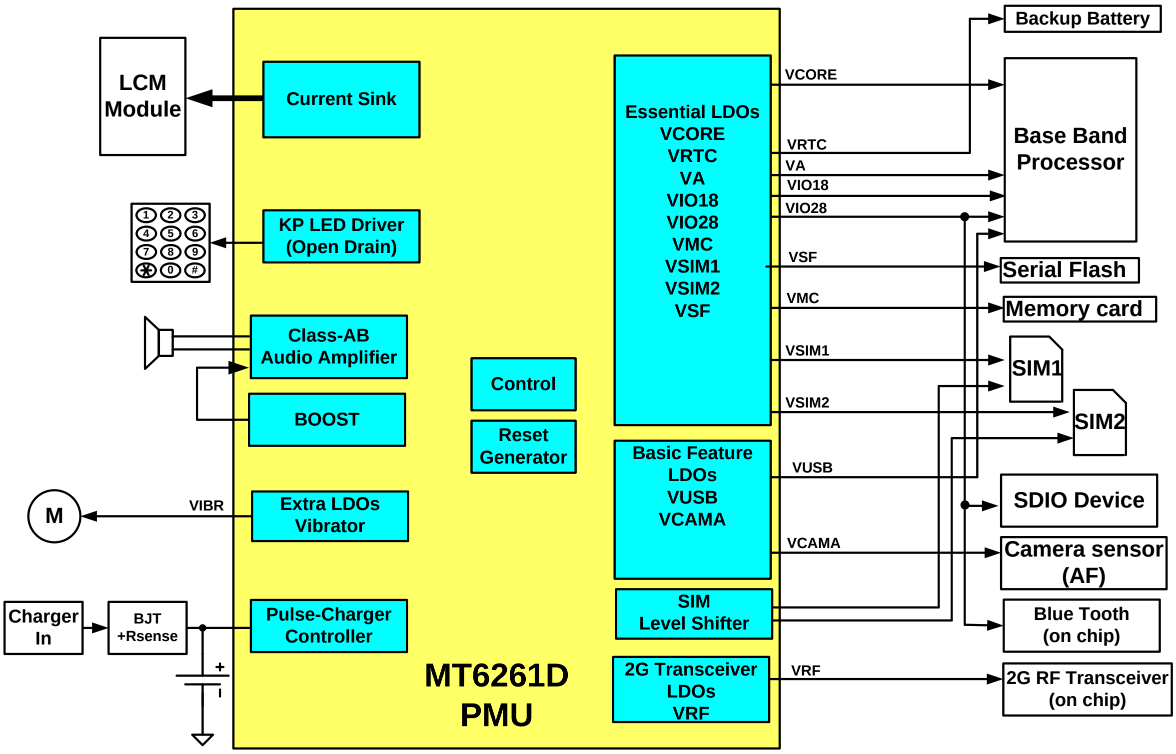

Figure 8. PMU system block diagram

2.6.1 LDO

PMU integrates 13 general low dropout regulators (LDO) optimized for their given functions by balancing the quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

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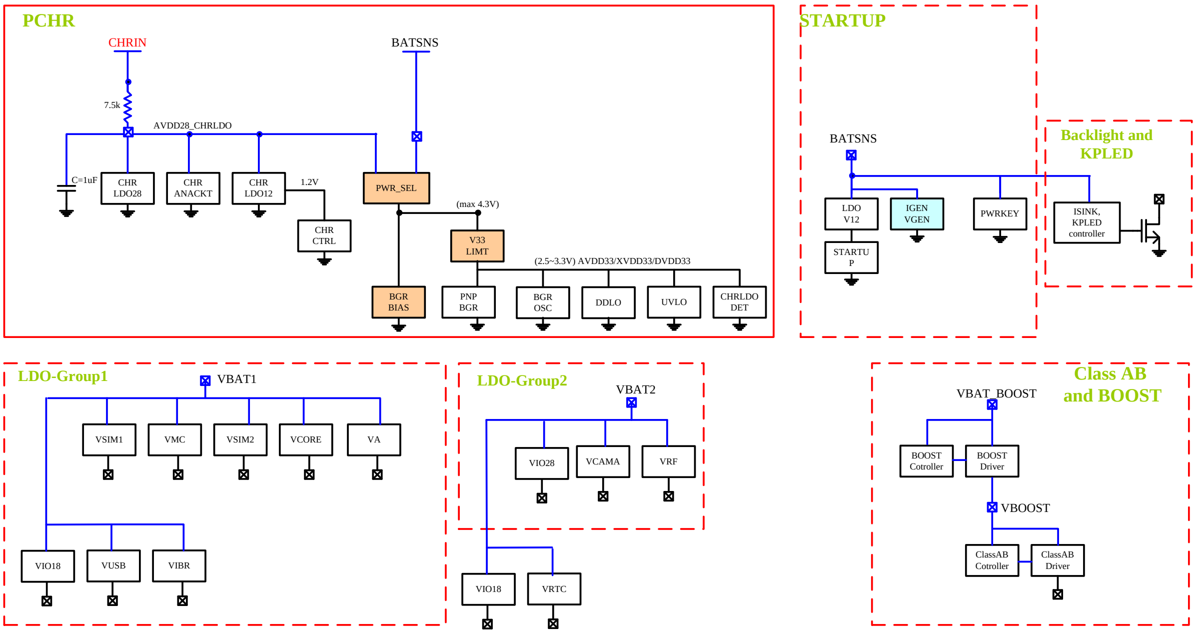

Figure 9. Power domain

2.6.1.1 LDO

A low-dropout regulator (LDO) is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to a very small difference between input and output voltages.

There are several features in the design of LDO, including discharge control, soft start and current limit. Before LDO is enabled, the output pin of LDO should be discharged first to avoid voltage accumulation on the capacitance. The soft-start limits inrush current and controls output-voltage rising time during the power-up. The current limit is the current protection to limit the LDO's output current and power dissipation.

There are three types of LDOs in PMU of MT6261D PMU. The analog LDO is optimized for low-frequency ripple rejection in order to reject the ripples coming from the burst of RF power amplifier. The digital IO LDO is a linear regulator optimized for very low quiescent current. The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features reverse current protection and is optimized for ultra-low quiescent current while sustaining the RTC function as long as possible.

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2.6.1.1.1 Block Description

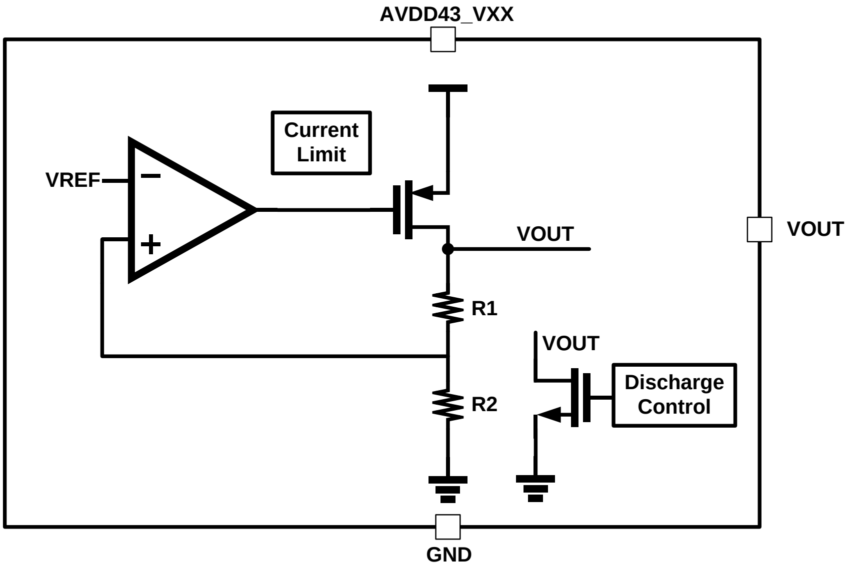

Figure 10. LDO block diagram

2.6.1.1.2 LDO Types

Table 21. LDO types and brief specifications

Type	LDO name	Vout (Volt)	Imax(mA)	Description
ALDO	VRF	2.8	150	RF chip and 26MHz reference clock
ALDO	VA	2.8	150	Analog baseband
ALDO	VCAMA	2.8	70	Camera sensor
DLDO	VIO28	2.8	100	Digital IO and Blue tooth
DLDO	VSIM1	1.8/3.0	30	SIM card
DLDO	VSIM2	1.8/3.0	30	SIM card
DLDO	VUSB	3.3	50	USB
DLDO	VIO18	1.8	100	Digital IO
DLDO	VCORE	0.75~1.35	150	Digital baseband
DLDO	VIBR	1.8/2.8/3.0	100	Vibrator
DLDO	VMC	1.8/2.8/3.0/3.3	100	Memory card
DLDO	VSF	1.86/2.8/3.0/3.3	50	Serial flash
RTCLDO	VRTC	2.8/3.3	2	Real-time clock

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2.6.1.1.3 Functional Specifications

Table 22. Analog LDO specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		μF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Includes load regulation, line regulation, and temperature coefficient	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Temperature coefficient				100	ppm/C
	PSRR	Iout < 0.5*Imax 10 < f < 3 kHz	65			dB
		Iout < 0.5*Imax 3K < f< 30 kHz	45			dB
	Output noise	With A-weighted filter			90	uVrms
	Quiescent current	Iout = 0		55		μA
	Turn-on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn-on settling time	Iout = 0			240	μsec

Table 23. Digital LDO specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1[5]		μF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Includes load regulation, line regulation, and temperature coefficient	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Temperature coefficient				100	ppm/C

[5] VCORE loading capacitor typical value is 2.2uF. Other LDOs are 1uF.

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Quiescent current	Iout = 0		30		μA
	Turn-on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn-on settling time	Iout = 0			240	μs

Table 24. RTC LDO specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		μF
	Vout	Includes load regulation, line regulation, and temperature coefficient	2	2.8	3	V
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout = 0		15		μA

2.6.2 BOOST

2.6.2.1 Functional Specifications

Table 25. RTC LDO specification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Cin Cout			2.2uF 4.7uF		μF
	L	Rdcr,max<80mOhm		0.68		uH
	Vout			5.3		V
	Ripple	Vin=3.4V/3.8V/4.2V, Cin=2.2uF & Cout=4.7uF, L= 0.68uH (Rdcr,max<80mOhm) 650mA , switching Freq 2MHz			100	mV
	Switching frequency			2		MHz
	Quiescent current	Iout = 0		4	6	mA

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2.6.3 ISINK and KPLED Switches

One built-in open-drain output switch drives the keypad LED (KPLED) in the handset. The switch is controlled by the baseband with enabling registers. The switch of keypad LED can sink as much as 60mA current, and the output is high impedance when disabled. The value of the sink current decides the brightness of the LED.

The current controlled open drain drivers are also implemented to drive the LCM backlight module, and provides currentfrom 4mA to 96mA.

2.6.3.1 Block Description

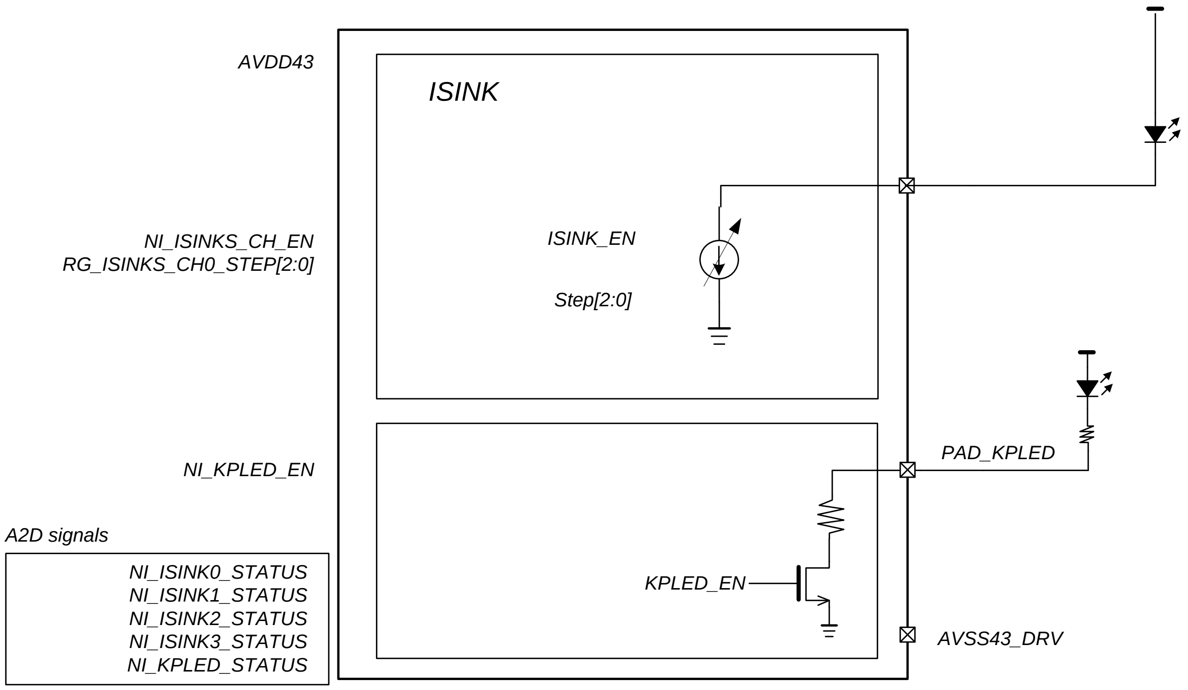

Figure 11. ISINKs and KPLED switches bock diagram.

2.6.3.2 Functional Specifications

Table 26. ISINKs and KPLED Switches Specification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Sink current of keypad LED driver	Von > 0.5V, 100% dimming duty	60			mA
	1 ch Sink current of ISINK without current	Von > 0.15V, 100% dimming duty,		4		mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	double option	ISINKS_CHx_STEP = 000				
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 001		8		mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 010		12		mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 011		16		mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 100		20		mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 101		24		mA
	Current mismatch	Von > 0.15V, 100% dimming duty	-5		5	%

2.6.4 STRUP

PMU handles the power-on and off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ 3.4V) nor in the thermal condition, there are three methods to power on the handset system: pulling PWRKEY low (the user pushes PWRKEY), pulling PWRBB high (baseband BB_WakeUp) or valid charger plug-in.

According to different battery voltage (VBAT) and phone states, control signals and regulators will have different responses.

2.6.5 PCHR

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector can resist higher input voltage than other parts of the PMU.

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2.6.5.1 Block Description

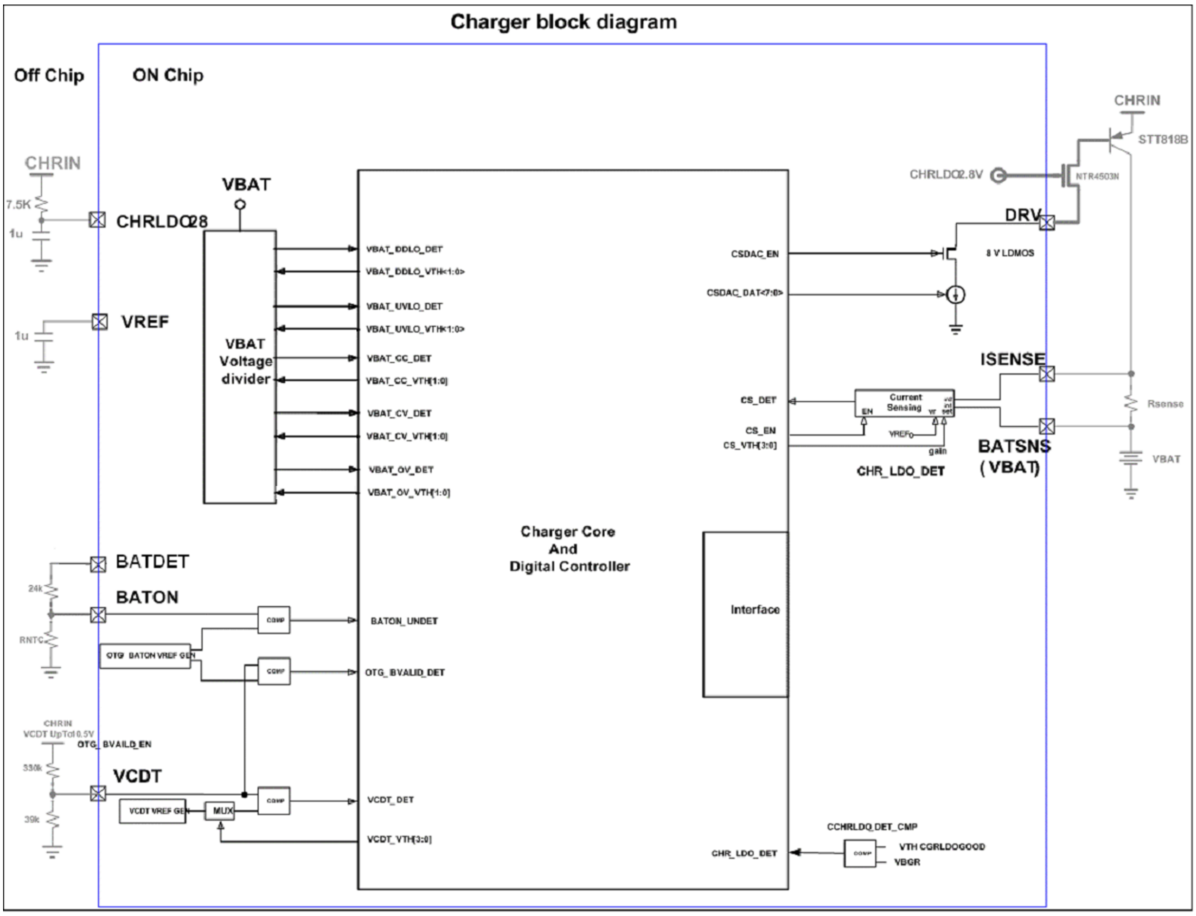

Figure 12. PCHR block diagram.

2.6.5.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0 V), the charger detector stops the charging process immediately to avoid burning out the chip or even the phone. In addition, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

2.6.5.1.2 Charging Control

When the charger is active, the charger controller manages the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.2V, PMU power-off state), CC mode (constant current mode or fast charging mode at the range 3.2V < VBAT < 4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery. The charging states diagram is shown in the figure below.

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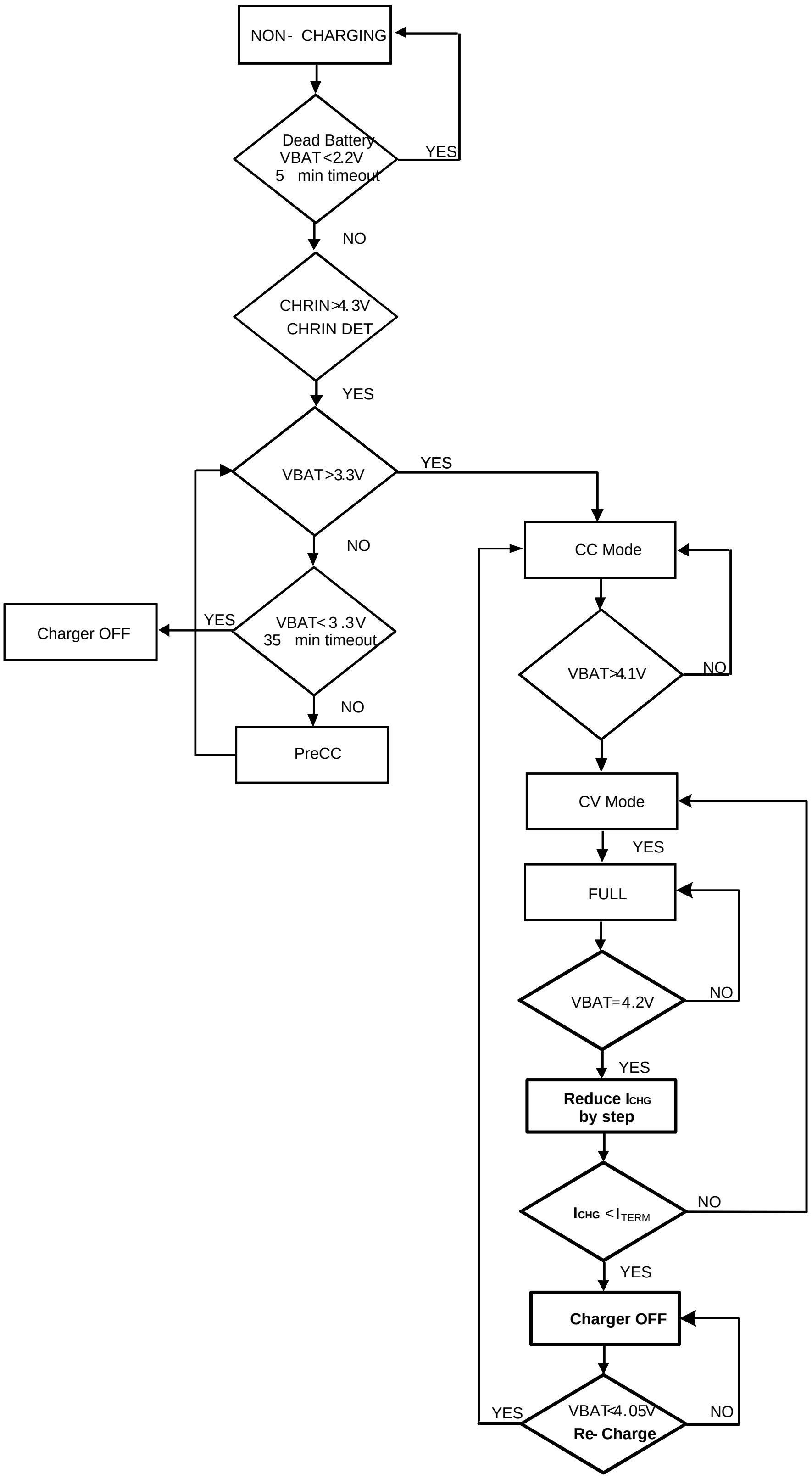

Figure 13. Charging states diagram

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Pre-charge mode

When the battery voltage is in the UVLO state, the charger operates in the pre-charge mode. There are two steps in this mode. When the battery voltage is deeply discharged below 2.2V, PRECC1 trickle charging current will be applied to the battery.

The PRECC1 trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, called the PRECC2 stage, the closed-loop pre-charge is enabled. The voltage drop across the external RSENSE is kept around 40mV (AC charger) or 14mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC2,AC\,adapter} = \frac{V_{SENSE}}{Rsense} = \frac{40mV}{Rsense}$$

$$I_{PRECC2,USB\,HOST} = \frac{V_{SENSE}}{Rsense} = \frac{14mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.4V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.2ohm, the CC mode charging current can be set from 70 to 800mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant voltage mode and over-voltage protection (OV)

While the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. While the battery voltage actually reaches 4.2V, the charging current is gradually decreased step-by-step, the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches zero automatically and this mechanism is optimized for different battery

BC1.1 Dead-Battery Support of China Standard

MT6261D supports dead-battery condition from China standard (called BC1.1). The specification protects dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after applying trickle current, the charger will be disabled. On the other hand, if the battery voltage is raised to above 2.2V, the charger will enter the PRECC2 stage, and the charging current will be 70mA or 200mA depending on the type of charging port.

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Under the condition of battery voltage from 2.2V to 3.3V, the charger will charge the battery with the PRECC2 current.

A dedicated 5mins (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35mins (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.3V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

2.6.5.2 Functional Specifications

Table 27. Charger detection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charger detect-on range		4.3		7	V

Table 28. Pre-charge specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	IUNIT with 500ms pulse	VBAT < 2.2V	20	48	100	mA
	Pre-charging current	VBAT < 2.2V (500ms pulse)	20	48	100	mA
		VBAT ≥ 2.2V (USB host)	$7/R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter < 7V)	$30/R_{sense}$	$40/R_{sense}$	$50/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter > 7V)	$7/R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
	Pre-charging off threshold	CHR_EN = L		3.3		V
	Pre-charging off hysteresis			0.4		V

Table 29. Constant current specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	CC mode charging current (CS_VTH)	CS_VTH [3:0] = 0000		$320/R_{sense}$		mA
		CS_VTH [3:0] = 0001		$300/R_{sense}$		mA
		CS_VTH [3:0] = 0010		$280/R_{sense}$		mA
		CS_VTH [3:0] = 0011		$260/R_{sense}$		mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		CS_VTH [3:0] = 0100		$240/R_{sense}$		mA
		CS_VTH [3:0] = 0101		$220/R_{sense}$		mA
		CS_VTH [3:0] = 0110		$200/R_{sense}$		mA
		CS_VTH [3:0] = 0111		$180/R_{sense}$		mA
		CS_VTH [3:0] = 1000		$160/R_{sense}$		
		CS_VTH [3:0] = 1001		$140/R_{sense}$		
		CS_VTH [3:0] = 1010		$130/R_{sense}$		
		CS_VTH [3:0] = 1011		$110/R_{sense}$		
		CS_VTH [3:0] = 1100		$90/R_{sense}$		
		CS_VTH [3:0] = 1101		$60/R_{sense}$		
		CS_VTH [3:0] = 1110		$40/R_{sense}$		
		CS_VTH [3:0] = 1111		$14/R_{sense}$		
	Current sensing resistor	RSENSE		0.2		ohm

Table 30. Constant voltage and over-voltage protection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charging complete threshold		4.15	4.2	4.25	V
	Battery over-voltage protection threshold (OV)			4.3		V

Table 31. BC1.1 specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
IUNIT	BC1.1 trickle current	VBAT < 2.2V		50	100	mA
IPRECC2 (USB host)	PRECC2 current	2.2 < VBAT < 3.3V		70	100	mA
IPRECC2 (AC adapter)	PRECC2 current	2.2 < VBAT < 3.3V		200	250	mA
T1	5 minute dedicated timer	2.2 < VBAT < 2.7V		5	6.5	min.
T2	35 minute dedicated timer	2.7 < VBAT < 3.3V		35	38.5	min.
TUNIT	BC1.1 trickle current period			550	770	ms.

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2.7 GSM/GPRS RF

2.7.1 General Description

2G RFSYS which is built in MT6261D SOC is a highly integrated RF transceiver for multi-band GSM and GPRS cellular systems.

The features include:

Receiver

- Single-end saw-less Rx
- Quadrature RF mixer
- Fully integrated channel filter
- High dynamic range ADC
- 12dB PGA gain with 6dB gain step

Transmitter

- High accurate transmitter modulator for GSM/GPRS application
- Built-in calibration of SX loop filter and loop gain

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GSM/GPRS applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26 MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning

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– On-chip programmable capacitor array for fine-tuning

– Supports 32K XTAL-less operation

2.7.2 Functional Block Diagram

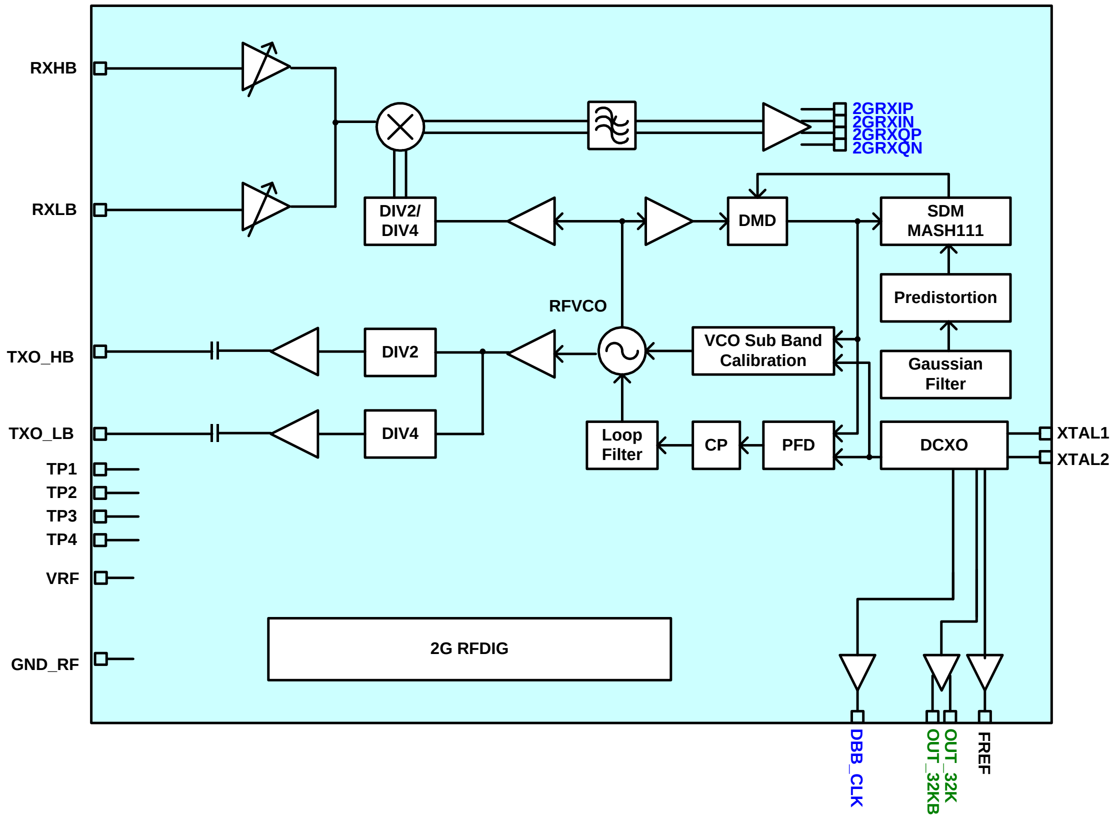

Figure 14. Diagram of MT6261D 2G RFSYS

2.7.3 Electrical Characteristics

Table 32. DC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

RFSYS mode	VRF	AVDD28_2GAFE	RFSYS total	Unit
BCM_Deep sleep (DCXO is off)	17	1	18	uA
BCM_Sleep (DCXO is on)	1.2	0.26	1.5	mA
Low power mode	60	1	61	uA
Full power mode	1.2	0.26	1.5	mA
RX (GSM850/EGSM)	62	5	67	mA
RX (DCS/PCS)	66	5	71	mA

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RFSYS mode	VRF	AVDD28_2GAFE	RFSYS total	Unit
TX (GSM850/EGSM)	41	2	43	mA
TX (DCS/PCS)	36	2	38	mA

Table 33. Rx AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Input frequency	F_{RX}	GSM850		869		894	MHz
		GSM900		925		960	MHz
		DCS1800		1,805		1,880	MHz
		PCS1900		1,930		1,990	MHz
Voltage gain 1	G_1	GSM850	LNA = High gain PGA = High gain	52[1]	55		dB
		GSM900		52[2]	55		dB
		DCS1800	LNA = High gain PGA = High gain	52[3]	55		dB
		PCS1900		52[4]	55		dB
Voltage gain 2	G_2	GSM850	LNA = Middle gain PGA = High gain		46		dB
		GSM900			46		dB
		DCS1800	LNA = Middle gain PGA = High gain		45		dB
		PCS1900			45		dB
Voltage gain 3	G_3	GSM850	LNA = Low gain PGA = High gain		26		dB
		GSM900			26		dB
		DCS1800	LNA = Low gain PGA = High gain		26		dB
		PCS1900			26		dB
Noise figure at 25°C	NF_{25}	GSM850	G_1		3	5[1]	dB
		GSM900			3	5[2]	dB
		DCS1800			3	5[3]	dB
		PCS1900			3	5[4]	dB
Noise figure at 85°C	NF_{85}	GSM850	G_1		4.5		dB
		GSM900			4.5		dB
		DCS1800			4.5		dB
		PCS1900			4.5		dB
2nd-order input intercept point	IIP2	GSM850	G2	31[1]	43		dBm
		GSM900		31[2]	43		dBm
		DCS1800		31[3]	43		dBm
		PCS1900		31[4]	43		dBm
3rd-order input intercept point	IIP3	GSM850	G2	-14[1]	-3		dBm
		GSM900		-14[2]	-3		dBm
		DCS1800		-14[3]	-3		dBm
		PCS1900		-14[4]	-3		dBm
3rd-order input intercept point @ -20°C	$IIP3_{-20}$	GSM850	G2		-5		dBm
		GSM900			-5		dBm
		DCS1800			-5		dBm

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Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
		PCS1900			-5		dBm
Receiver S/N with 3MHz blocker	SN_{3M}	GSM850	G2 Blocker = -23dBm	8[1]	12		dB
		GSM900		8[2]	12		dB
		DCS1800	G2 Blocker = -26dBm	8[3]	12		dB
		PCS1900		8[4]	12		dB
Receiver S/N with OBB	SN_{OOB}	GSM850	G2 Blocker = 2dBm, offset +/-20MHz	6[5]	8		dB
		GSM900		6[5]	8		dB
		DCS1800	G2 Blocker = -10/2dBm, offset +/-80/-100MHz	6[5]	8		dB
		PCS1900		6[5]	8		dB
Image rejection ratio	IRR	ALL	G2	32[1,2,3,4]	40		dB
Receiver channel response attenuation		ALL	@3MHz offset		20		dB
			@6MHz offset		35		dB
Receiver filtering 3-dB bandwidth		ALL	For all gain settings		900		kHz
PGA gain linearity		ALL	INL		0.2	1[5]	dBΩ
			DNL		0.1	0.5[5]	dBΩ
PGA gain step		ALL			6		dBΩ
PGA dynamic range		ALL			12		dBΩ
I/Q common-mode output voltage		ALL	G1	1.1[5]	1.2	1.3[5]	V
Output static dc offset		ALL	G1		100	200	mV

Table 34. Tx GMSK AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Frequency	F_{TX}	GSM850		824		849	MHz
		GSM900		880		915	MHz
		DCS1800		1,710		1,785	MHz
		PCS1900		1,850		1,910	MHz
RMS phase error	PE_{rms}	GSM850 GSM900			1.5	2.5[1,2]	degree
		DCS1800 PCS1900			1.5	2.5[3,4]	degree
Output modulation spectrum	ORFS	GSM850 GSM900	400kHz offset (RBW = 30kHz bandwidth)		-66	-64[1,2]	dBc
		DCS1800 PCS1900			-66	-64[3,4]	dBc
		GSM850 GSM900	1.8MHz offset (RBW = 30kHz bandwidth)			-75[5]	dBc
		DCS1800 PCS1900				-75[5]	dBc

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Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Tx noise in Rx band		GSM850	20MHz offset		-165	-163[5]	dBc/Hz
			35MHz offset		-166	-164[5]	dBc/Hz
		GSM900	20MHz offset		-165	-163[5]	dBc/Hz
			35MHz offset		-166	-164[5]	dBc/Hz
		DCS1800	20MHz offset		-160	-156[5]	dBc/Hz
		PCS1900	20MHz offset		-160	-156[5]	dBc/Hz
Output power level	P_{out}	GSM850 GSM900	PA driver amplifier R_{load} = 50Ω	1[1,2]	3	6[1,2]	dBm
		DCS1800 PCS1900		1[3,4]	3	6[3,4]	dBm
Output 3rd harmonics		ALL	PA driver amplifier		-10		dBc

Table 35. SX AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Frequency range	F_{range}		3,296		3,980	MHz
Reference frequency	F_{ref}			26		MHz
Frequency step resolution	F_{res}			3		Hz
Phase noise	PN_{10k}	@ 10kHz offset		-83		dBc/Hz
	PN_{400k}	@ 400kHz offset		-114		dBc/Hz
	PN_{3M}	@ 3MHz offset		-136		dBc/Hz
Lock time of Rx burst	T_{lock_rx}	Frequency error < ± 0.1ppm		150	200[5]	us
Lock time of Tx burst	T_{lock_tx}	Frequency error < ± 0.1ppm		200	300[5]	us
Pushing figure		With internal RFVCO LDO		400		kHz/V

Table 36. DCXO AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating frequency	F_{ref}			26		MHz
Crystal C load	C_L			7.5		pF
Crystal tuning sensitivity	T_S		27.5	32.3		ppm/pF
Static range	SR	CDAC from 0 to 255	± 22	± 50		ppm
Dynamic range	DR	CAFC from 0 to 8191	36	50		ppm
AFC tuning step	$F_{res\text{-}AFC}$			0.008		ppm/DAC
AFC settling time	T_{AFC}	CAFC from 0 to 8191 CAFC from 8191 to 0 Frequency error < 0.1ppm		100	200[5]	us
Start-up time	T_{DCXO}	Frequency error < 1ppm Amplitude > 90 %			4[5]	ms
Pushing figure				0.2		ppm/V

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Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Fref buffer output level	V_{Fref}	Max. loading = 19pF	0.8[5]			V_{p-p}
Fref buffer output phase noise		10kHz offset Jitter noise		-135		dBc/Hz

[1, 2]: Tested at E-GSM Tx channel 0 and GSM850 Rx channel 190.

[3, 4]: Tested at PCS Tx channel 601 and DCS Rx channel 636.

[5]: Not subject to production test – verified by characterization and design.

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2.8 Bluetooth

2.8.1 Block Description

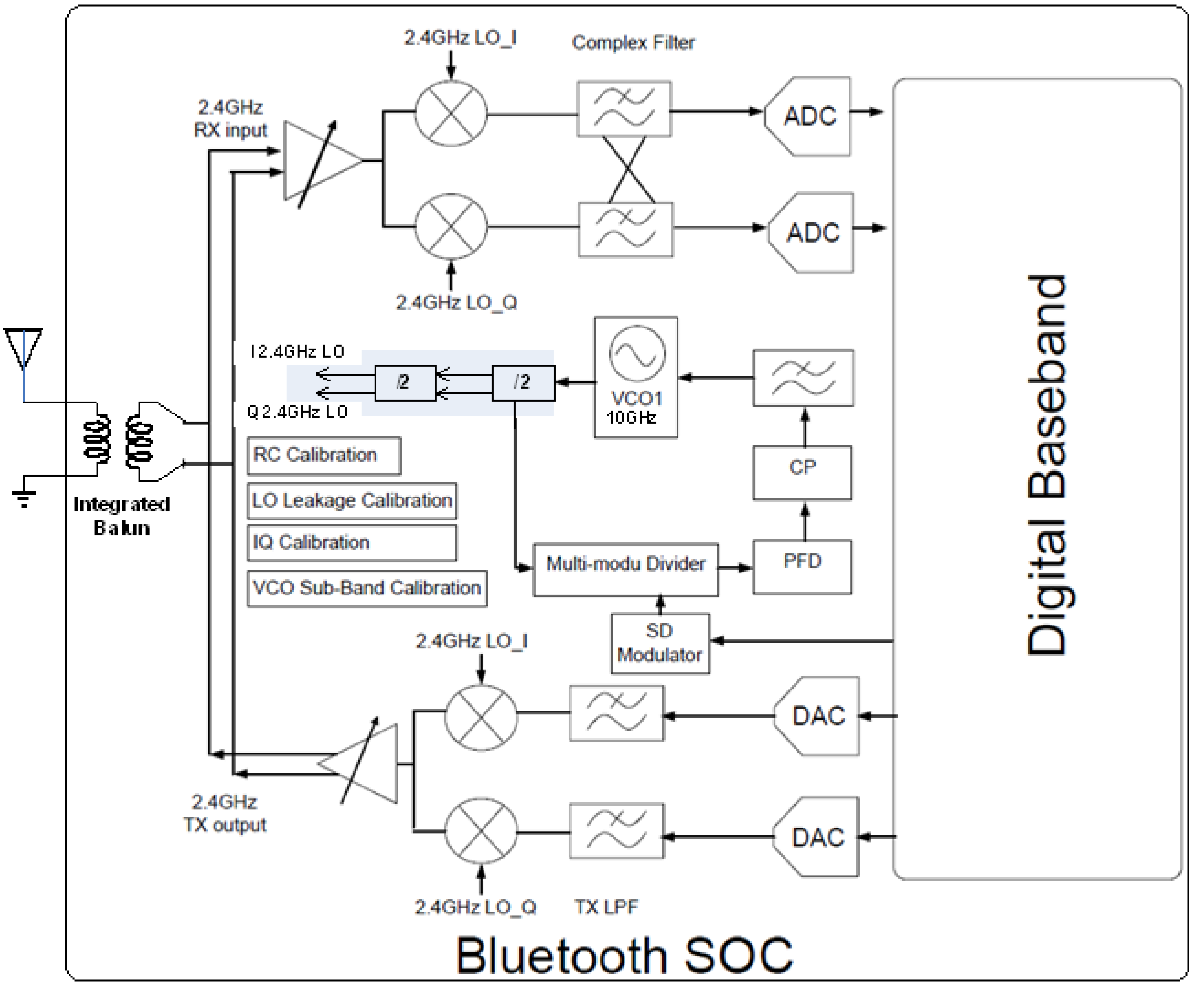

Figure 15. System diagram of Bluetooth RF transceiver

The Bluetooth RF subsystem contains a fully integrated transceiver.

For TX path, the baseband transmit data are digitally modulated in the baseband processor then up-converted to 2.4GHz RF channels through DA converter, filter, IQ up-converter and power amplifier. The power amplifier is capable of transmitting 7.5dBm power for class-1 operation.

For RX path, MT6261D is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with LO from the synthesizer, which supports different clock frequencies as the reference clock. The mixer output is then converted to digital signal and down-converted to baseband

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for demodulation. A fast AGC enables effective discovery of device within dynamic range of the receiver.

MT6261D features self calibration schemes to compensate the process and temperature variation to maintain high performance. Those calibrations are performed automatically right after system boot-up.

2.8.2 Functional Specifications

2.8.2.1 Basic Data Rate – Receiver Specifications

Table 37. Basic data rate – receiver specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	BER < 0.1%	-	-95	-	dBm
	Max. detectable input power	BER < 0.1%	-	0	-	dBm
	C/I co-channel selectivity	BER < 0.1%	-	4	-	dB
	C/I 1 MHz adj. channel selectivity	BER < 0.1%	-	-12	-	dB
	C/I 2 MHz adj. channel selectivity	BER < 0.1%	-	-42.5	-	dB
	C/I ≥ 3 MHz adj. channel selectivity	BER < 0.1%	-	-46	-	dB
	C/I image channel selectivity	BER < 0.1%	-	-24	-	dB
	C/I image 1 MHz adj. channel selectivity	BER < 0.1%	-	-45	-	dB
	Out-of-band blocking	30 to 2,000 MHz	-	-4	-	dBm
		2,000 to 2,399 MHz	-	-18	-	dBm
		2,498 to 3,000 MHz	-	-18	-	dBm
		3,000 MHz to 12.75 GHz	-	1	-	dBm
	Intermodulation		-	-22	-	dBm

2.8.2.2 Basic Data Rate – Transmitter Specification

Table 38. Basic data rate – transmitter specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Maximum transmit power		-	7.5	-	dBm
	Gain step		-	4	-	dB
	Δf1avg (00001111)		140	158	175	kHz
	Δf2max (10101010)		115	130	-	kHz
	Δf1avg/Δf2avg		0.8	0.9	-	kHz

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Initial carrier frequency drift		-75	5	75	kHz
	Frequency drift	DH1	-25	9	25	kHz
		DH3	-40	10	40	kHz
		DH5	-40	10	40	kHz
	Max. drift rate		-	100	400	Hz/µs
	BW_{20dB} of Tx output spectrum		-	920	1,000	kHz
	In-band spurious emission	±2 MHz offset	-	-38	-	dBm
		±3 MHz offset	-	-43	-	dBm
		> ±3 MHz offset	-	-43	-	dBm
	Out-of-band spurious emission	30 MHz to 1 GHz	-	-36	-	dBm
		1 to 12.75 GHz	-	-30	-	dBm
		1.8 to 1.9 GHz	-	-47	-	dBm
		5.15 to 5.3 GHz	-	-47	-	dBm

2.8.2.3 Enhanced Data Rate – Receiver Specifications

Table 39. Enhanced data rate – receiver specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	π/4 DQPSK, BER < 0.01%	-	-95	-	dBm
		8PSK, BER < 0.01%	-	-88	-	dBm
	Max. detectable input power	π/4 DQPSK, BER < 0.01%	-	-4.5	-	dBm
		8PSK, BER < 0.01%	-	-4.5	-	dBm
	C/I co-channel selectivity	π/4 DQPSK, BER < 0.01%	-	8	-	dB
		8PSK, BER < 0.01%	-	14.5	-	dB
	C/I 1MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-13	-	dB
		8PSK, BER < 0.01%	-	-7	-	dB
	C/I 2MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-42	-	dB
		8PSK, BER < 0.01%	-	--41.5	-	dB
	C/I ≥ 3MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-48	-	dB
		8PSK, BER < 0.01%	-	-44.5	-	dB
	C/I image channel selectivity	π/4 DQPSK, BER < 0.01%	-	-30	-	dB
		8PSK, BER < 0.01%	-	-23	-	dB
	C/I image 1 MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-47.5	-	dB
		8PSK, BER < 0.01%	-	-44.5	-	dB

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2.8.2.4 Enhanced Data Rate – Transmitter Specifications

Table 40. Enhanced data rate – transmitter specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Max. transmit power	π/4 DQPSK	-	4.5	-	dBm
		8PSK	-	4.5	-	dBm
	Relative transmit power	π/4 DQPSK	-	-1.7	-	dB
		8PSK	-	-1.7	-	dB
	Freq. stability ω_0	π/4 DQPSK	-	1.5	-	kHz
		8PSK	-	1.5	-	kHz
	Freq. stability ω_1	π/4 DQPSK	-	3	-	kHz
		8PSK	-	3	-	kHz
	$\lvert \omega_0+\omega_1 \rvert$	π/4 DQPSK	-	2.8	-	kHz
		8PSK	-	2.8	-	kHz
	RMS DEVM	π/4 DQPSK	-	7	-	%
		8PSK	-	6	-	%
	99% DEVM	π/4 DQPSK	-	11	-	%
		8PSK	-	11	-	%
	Peak DEVM	π/4 DQPSK	-	18	-	%
		8PSK	-	18	-	%
	In-band spurious emission	π/4 DQPSK, ±1 MHz offset	-	-28	-	dBm
		8PSK, ±1 MHz offset	-	-28	-	dBm
		π/4 DQPSK, ±2 MHz offset	-	-25	-	dBm
		8PSK, ±2 MHz offset	-	-25	-	dBm
		π/4 DQPSK, ±3 MHz offset	-	-40.5	-	dBm
		8PSK, ±3 MHz offset	-	-40.5	-	dBm

Note: To meet the specifications, use a front-end band-pass filter.

2.9 FM RF

2.9.1 Block Description

The connection between internal modules, as well as external interfaces, are as shown in Figure 16. The FM receiver section incorporates the complete receiving path with wide tuning range. The FM baseband signal processor incorporates the digital demodulator and audio processing function which provides superior audio quality.

FM contains completely integrated FM audio receiver functions (RDS/RBDS may also be supported depending on the model number). The integrated receiver enables superior sensitivity, ACI performance and FM audio performances with minimum external BOM.

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The FM subsystem supports either high performance stereo analog line out or digital audio output (I2S).
For models supporting RDS/RBDS, large dedicated internal data buffers are allocated to reduce the frequency of the interrupt to the host, so that the receiving host can enter low power states efficiently.

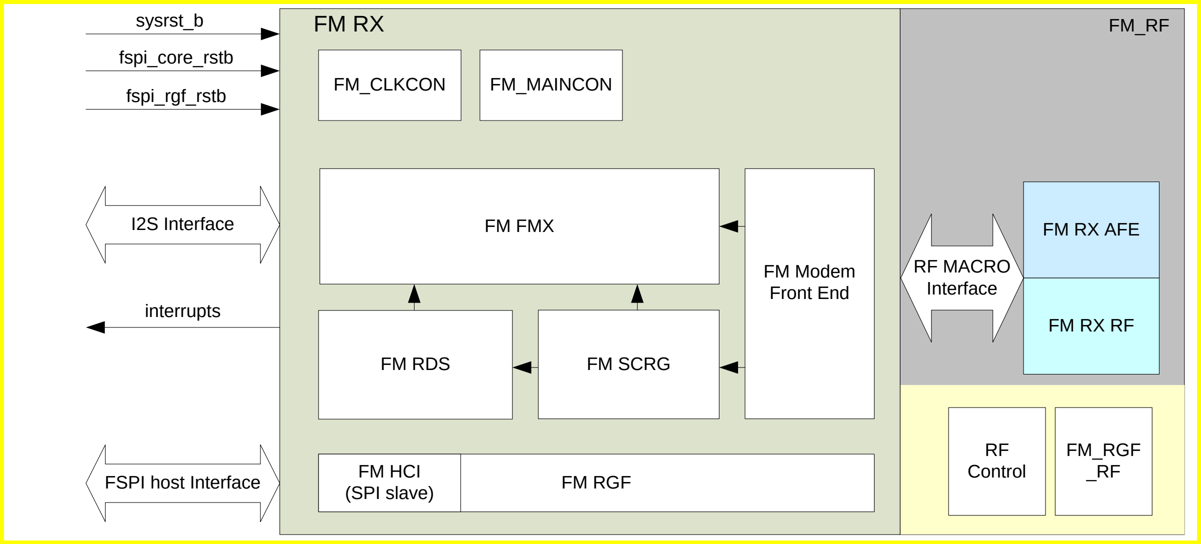

Figure 16. Block diagram of hardware top-level architecture

2.9.2 Functional Specifications

Table 41. FM receiver DC characteristics (TA=25°C, VDD=2.8V unless otherwise stated)

Operating mode	Current consumption	Unit
Idle	5	μA
FM receiver	12	mA

Unless otherwise stated, all receiver characteristics are applicable to both long and short antenna ports when operated under the recommended operating conditions. Typical specifications are for channel 98.7MHz, default register settings and under recommended operating conditions. The minimum and maximum specifications are for extreme operating voltage and temperature conditions, unless otherwise stated.

Table 42. FM receiver AC characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Input frequency range		65		108	MHz
	Sensitivity (long antenna)[1,3]	SINAD = 26dB, unmatched		3		dBμVemf
		SINAD = 26dB, matched		2		dBμVemf

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	RDS sensitivity (long antenna)	Δf=2kHz, BLER < 5%, unmatched		18		dBμVemf
	Sensitivity (short antenna)[1,3]	SINAD = 26dB, unmatched		3		dBμVemf
	RDS sensitivity (short antenna)	Δf = 2kHz, BLER < 5%, unmatched		18		dBμVemf
	LNA input resistance[4]	Antenna port		2.4k		Ohm
	LNA input capacitance[4]	Antenna port		8		pF
	AM suppression[1,4]	M = 0.3		58		dB
	Adjacent channel selectivity[1,4]	±200kHz		53		dB
	Alternate channel selectivity[1,4]	±400kHz		65		dB
	Spurious response rejection[4]	In-band		55		dB
	Maximum input level			117		dBμVemf
	Audio mono (S+N+D)/(N+D)[1,3,4]			60		dB
	Audio stereo (S+N+D)/(N+D)[2,3,4]			52		dB
	Audio stereo separation[4]	Δf = 75kHz		45		dB
	Audio output load resistance	Single-ended at AFR/AFL outputs		10k		Ohm
	Audio output load capacitance	Single-ended at AFR/AFL outputs		12.5		pF
	Audio output voltage[1,4]	At AFR/AFL outputs		80		mVrms
	Audio output THD[1,4]			0.05	0.1	%
	Audio output frequency range	3dB corner frequency	30		15k	Hz

[1] Δf = 22.5kHz, fm = 1kHz, 50μs de-emphasis, mono, L = R
[2] Δf = 22.5kHz, fm = 1kHz, 50us de-emphasis, stereo
[3] A-weighting, BW = 300 Hz to 15 kHz
[4] Vin = 60dBμVemf
[5] Reference clock accuracy assumes ideal FM source. If the input FM source has less frequency error, it is recommended to use a reference clock of accuracy within ±100ppm so as not to affect the channel scan quality.

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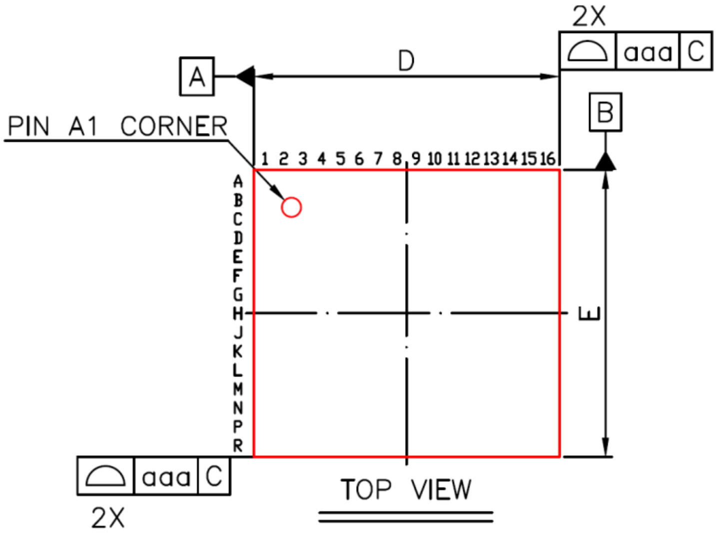
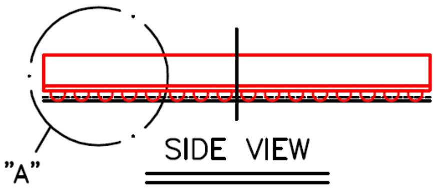
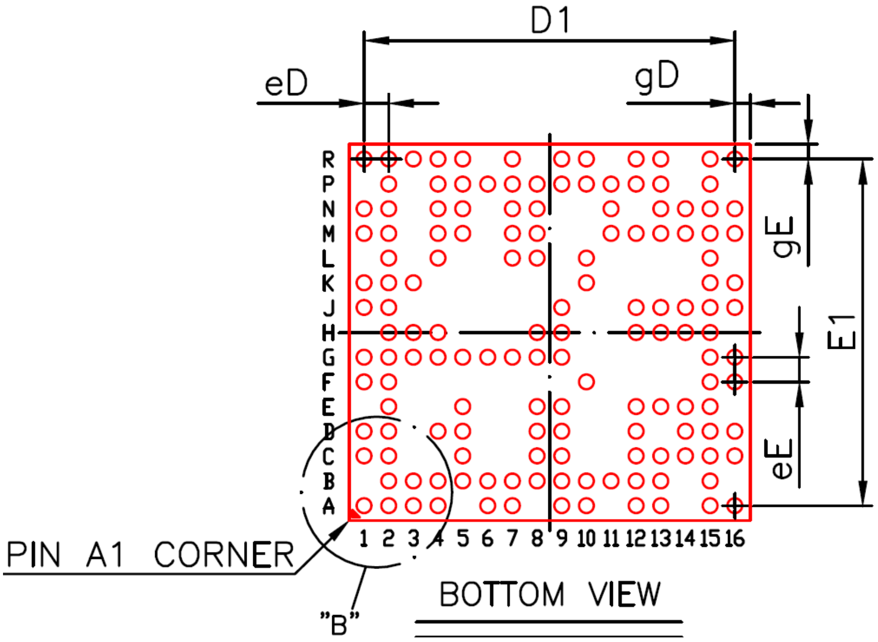
2.10 Package Information

2.10.1 Package Outlines







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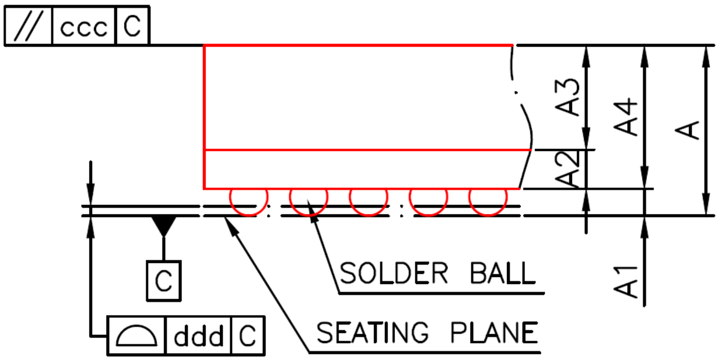

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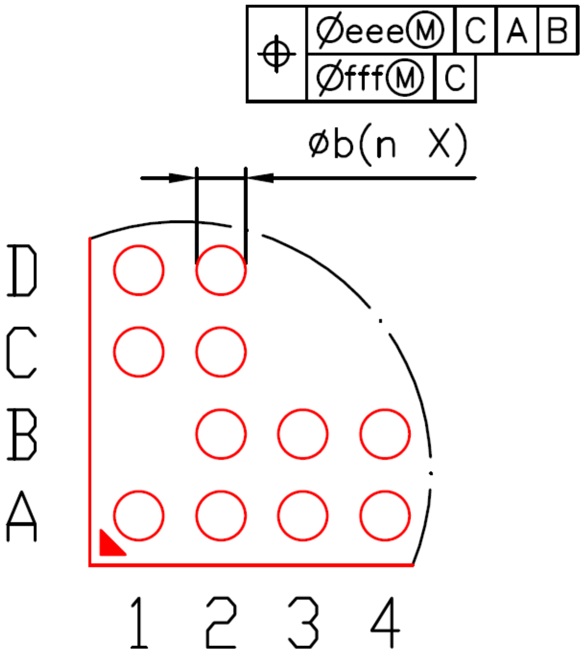

DETAIL : "B"

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Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	8.00	8.10	8.20
	Y	E	7.50	7.60	7.70
Ball Pitch	X	eD	0.50		
	Y	eE	0.50		
Mold Thickness		A3	0.65 Ref.		
Substrate Thickness		A2	0.11 Ref.		
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.05
Ball Diameter			0.30		
Ball Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa	0.10		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	145		
Edge Ball Center to Center	X	D1	7.50		
	Y	E1	7.00		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

Figure 17. Outlines and dimension of TFBGA 8.1mm*7.6mm, 145-ball, 0.5 mm pitch package

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2.10.2 Thermal Operating Specifications

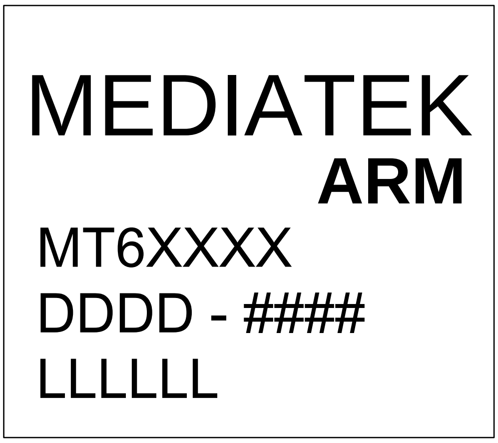
Symbol	Description	Value	Unit	Notes
	Thermal resistance from device junction to package case	48	C/W	
	Maximum package temperature	65	Deg C	
	Maximum power dissipation	1.28	W	

2.10.3 Lead-free Packaging

MT6261D is provided in a lead-free package and meets RoHS requirements

2.11 Ordering Information

2.11.1 Top Marking Definition



MTXXXXXX Product No.
DDDD: Date Code
####: Subcontractor Code
LLLLLL: Die Lot No.

Figure 18. Mass production top marking of MT6261D

Part number	Package	Description
MT6261DA/A	TFBGA	8.1mm*7.6mm, 145-ball, 0.5 mm pitch package, non-security version

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